

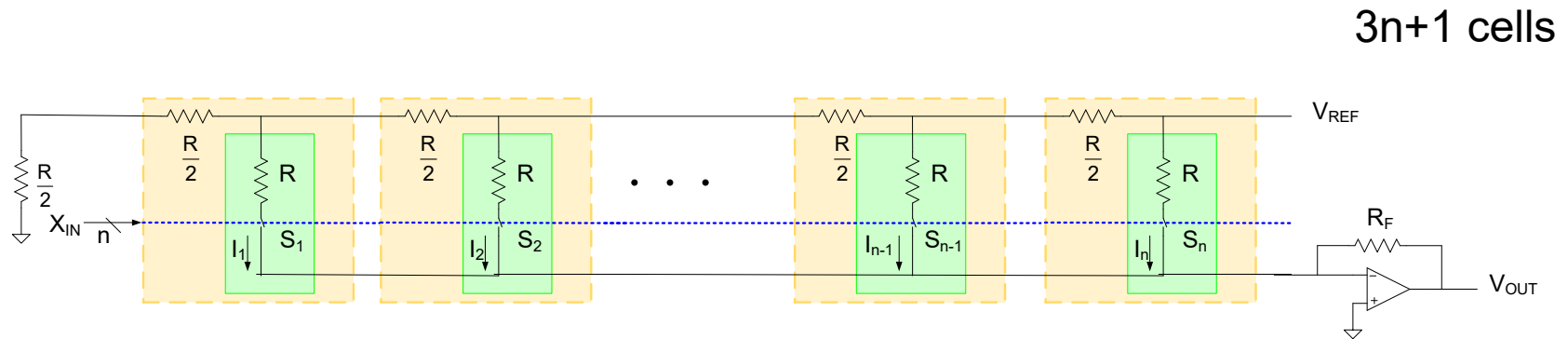
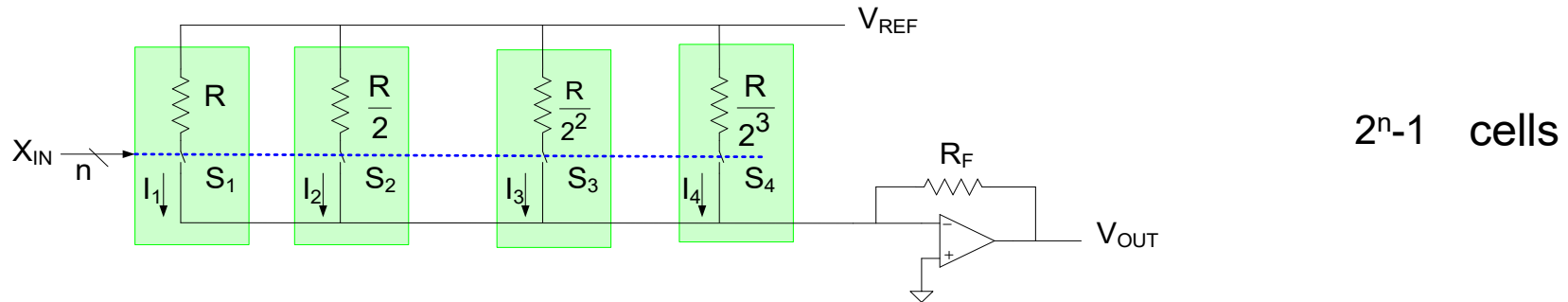
# EE 505

## Lecture 17

### Current Steering DACs

# Current Steering DACs

## Reduced Resistance Structure



Is the R-2R structure smaller ?

Does the R-2R structure perform better?

What metric should be used for comparing performance?

## Performance of Thermometer Coded vs Binary Coded DACs

### Conventional Wisdom:

- Thermometer-coded structures have inherently small DNL
- Binary coded structures can have large DNL
- INL of both structures is comparable for same total area (provided area appropriately allocated)

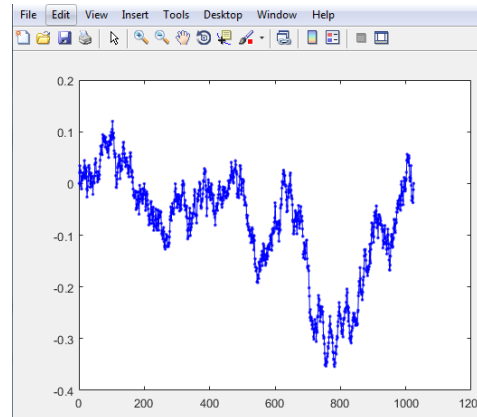
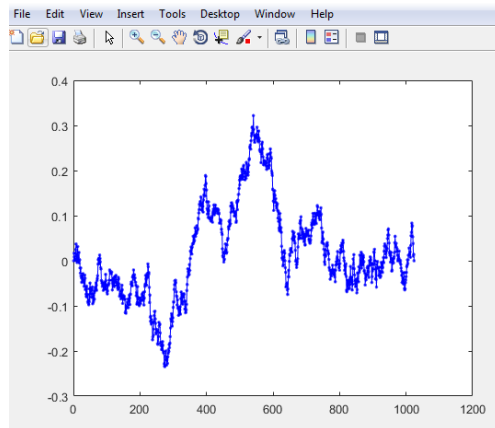
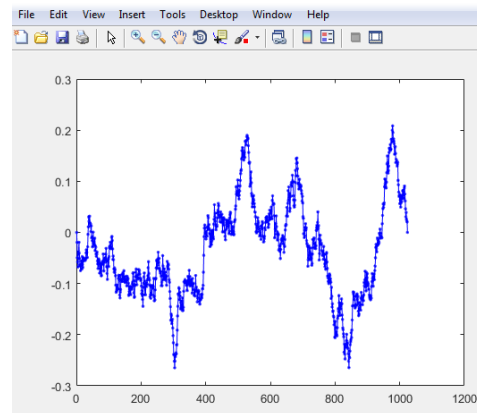
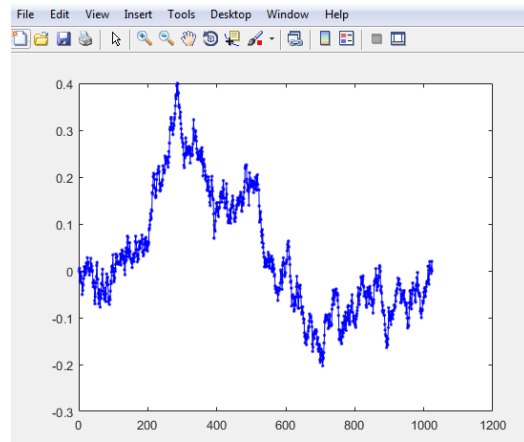
# Comparison of Thermometer Coded and Binary Coded DACs

Example:  $n=10$   
String DAC

$$A_R = 0.02 \mu\text{m}$$
$$R_N = 1\text{K}$$



Resistor Sigma =  $14.14 \Omega$



Low DNL and random walk nature should be apparent

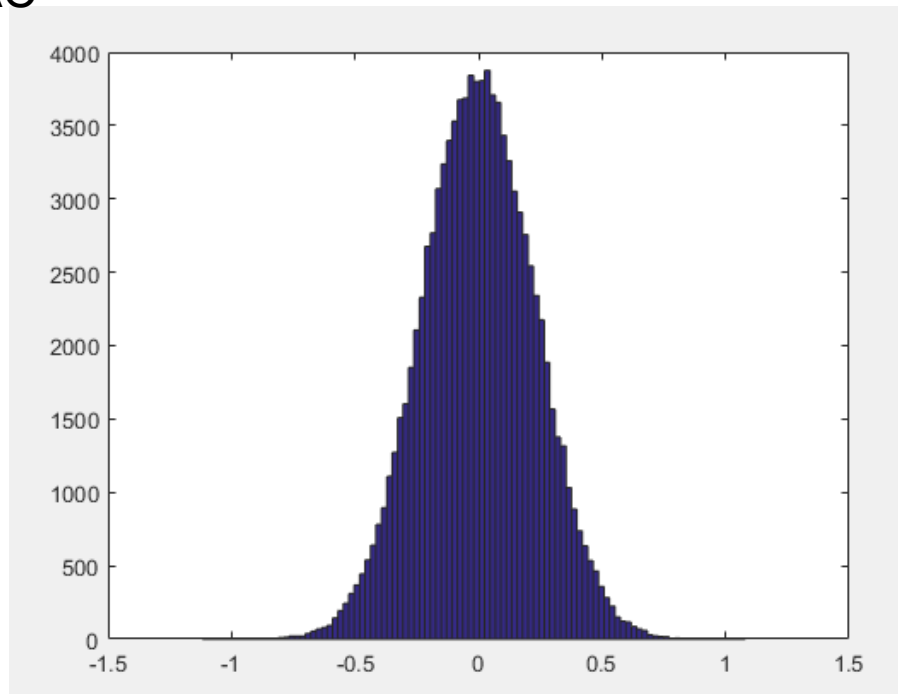
# Comparison of Thermometer Coded and Binary Coded DACs

Example:  $n=10$   
String DAC

$A_R=0.02\mu\text{m}$   
 $R_N=1\text{K}$



Resistor Sigma =  $14.14\ \Omega$



INLkmax\_mean =  $-2.11116\text{e-}05$

INLkmax\_sigma =  $0.226783$

Histogram of  $\text{INL}_{\text{kmax}}$  from 100,000 runs

Appears to be Gaussian

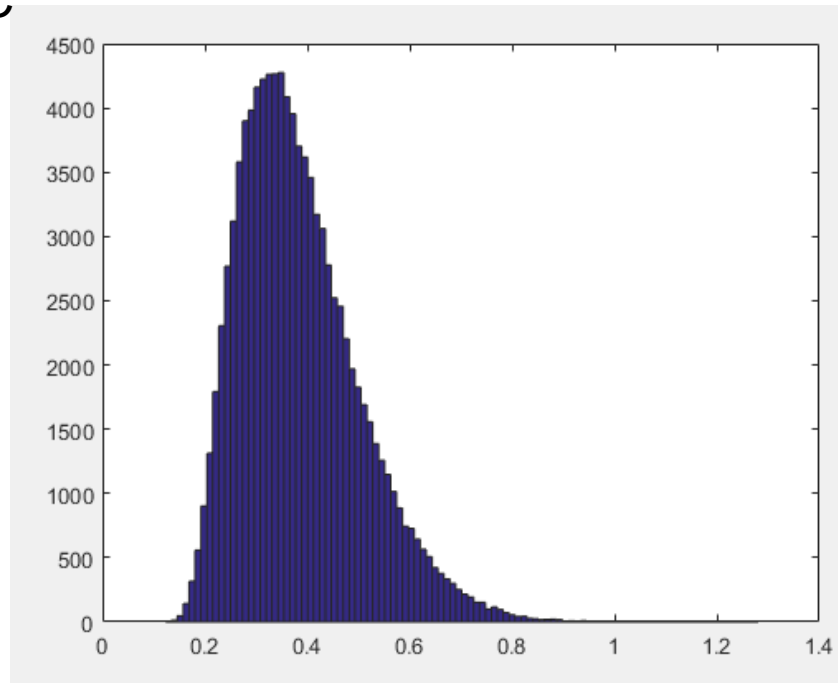
# Comparison of Thermometer Coded and Binary Coded DACs

Example:  $n=10$   
String DAC

$A_R=0.02\mu\text{m}$   
 $R_N=1\text{K}$



Resistor Sigma =  $14.14\ \Omega$



INLmean = 0.384382  
INLsigma = 0.117732

Histogram of INL from 100,000 runs

Not Gaussian

# Comparison of Thermometer Coded and Binary Coded DACs

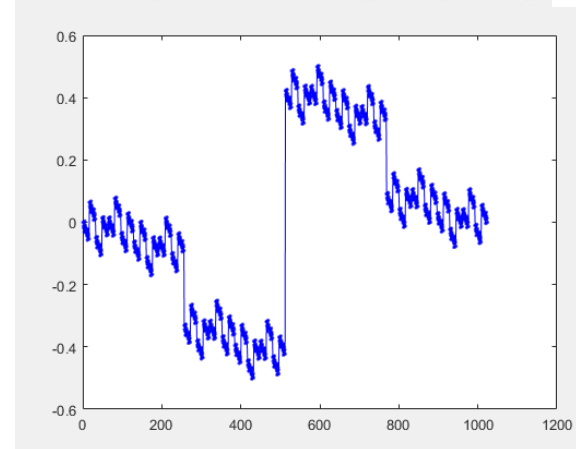
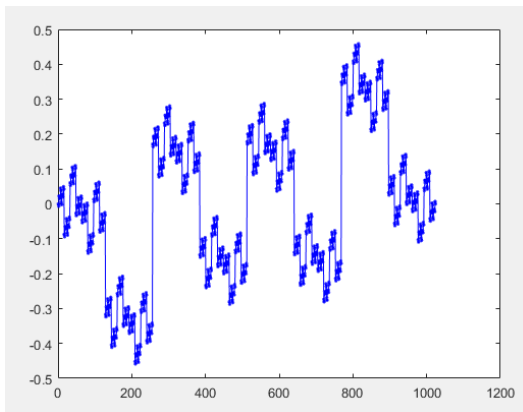
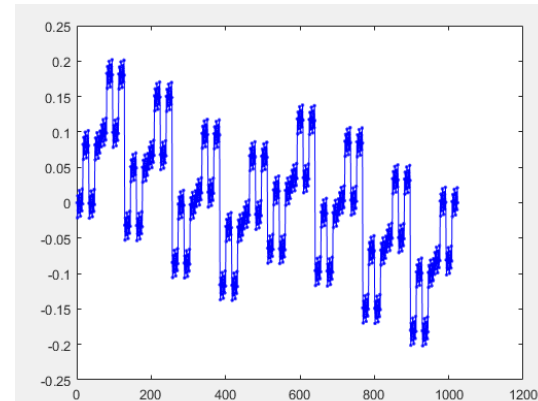
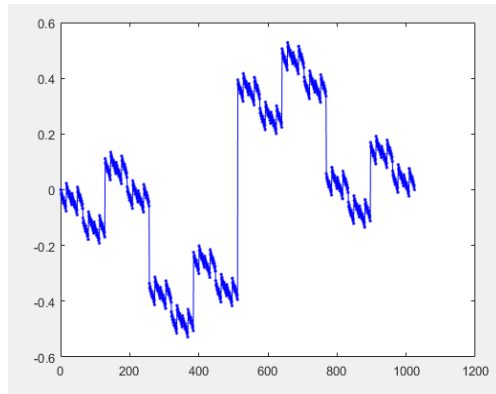
Example:  $n=10$



Resistor Sigma= 14.14  $\Omega$

Binary DAC

$A_R=0.02\mu\text{m}$   
 $R_N=1\text{K}$



Large DNL bit INL does not appear to be much different than for string DAC

# Comparison of Thermometer Coded and Binary Coded DACs

Example:  $n=10$

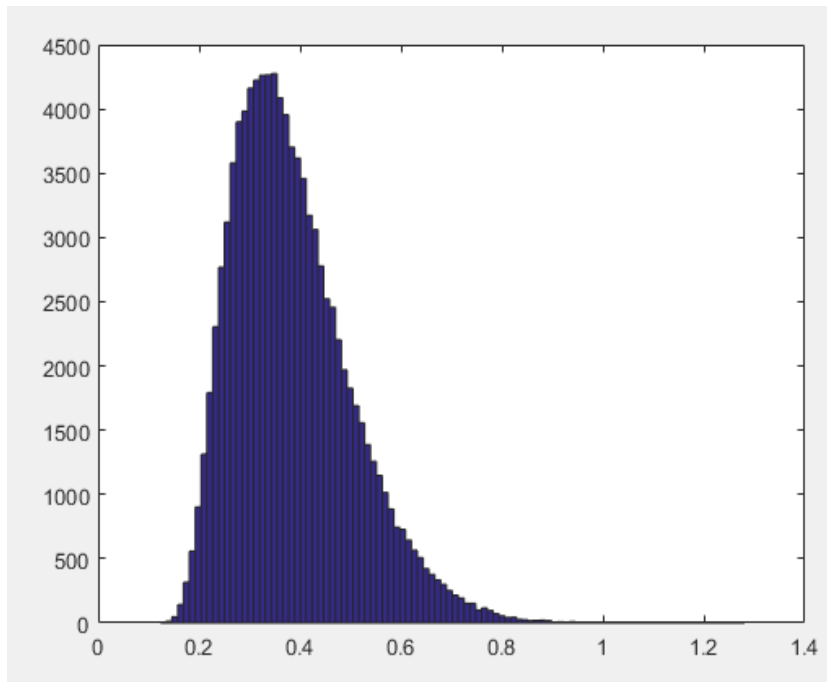
$A_R=0.02\mu\text{m}$   
 $R_N=1\text{K}$



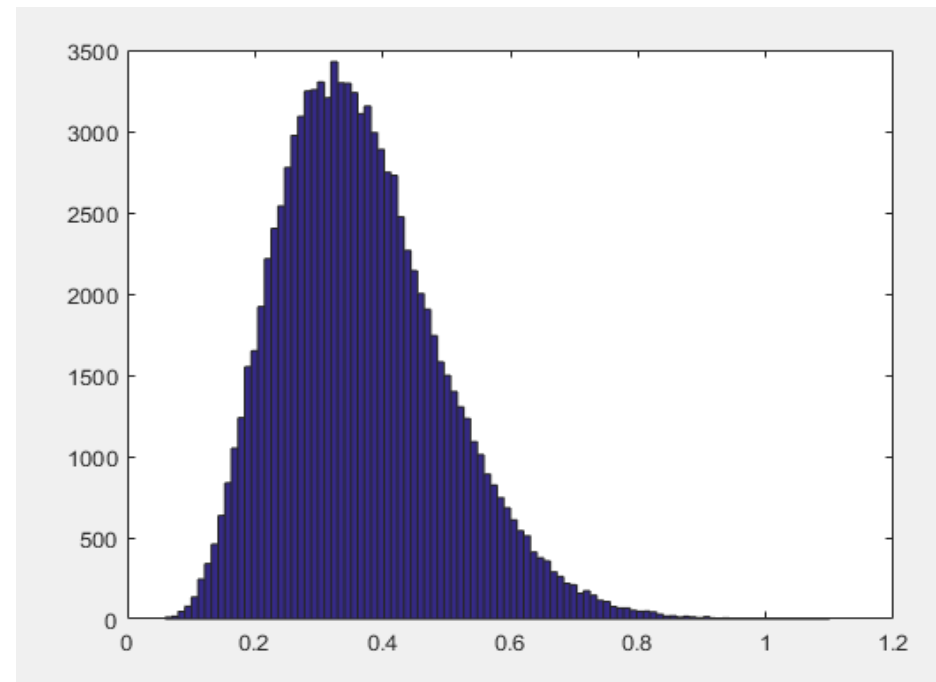
Resistor Sigma=  $14.14\ \Omega$

Both structures have essentially the same area

String DAC



Binary DAC



Histogram of INL from 100,000 runs

Since mathematical form for PDF is not available, not easy to analytically calculate yield



# Comparison of Thermometer Coded and Binary Coded DACs

Example:  $n=10$

$A_R=0.02\mu\text{m}$   
 $R_N=1\text{K}$



Resistor Sigma =  $14.14\ \Omega$

Both structures have essentially the same area

## String DAC

Resolution = 10       $AR = 0.02$   
Rnom = 1000      Area Unit Resistor =  $2\mu\text{m}^2$   
INLkmax\_mean =  $-2.11116\text{e-}05$   
INLmean = 0.384382  
INLtarget = 0.5000

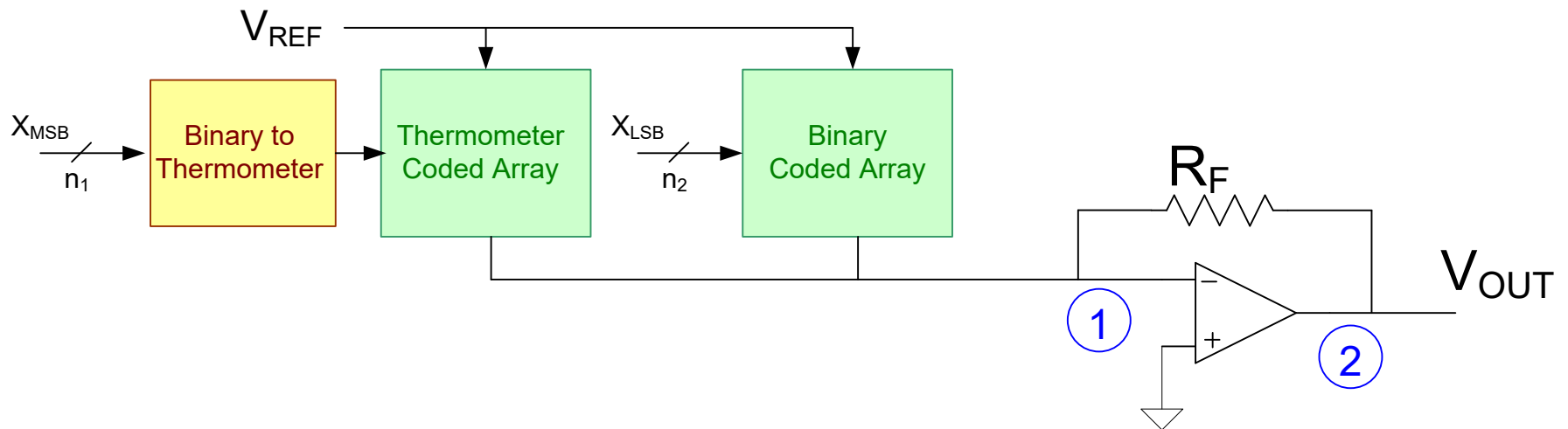
Nruns = 100000  
 Resistor Sigma = 14.1421  
INLkmax\_sigma = 0.226783  
INLsigma = 0.117732  
 Yield(%) = 84.0120

## Binary DAC

Resolution = 10       $AR = 0.02$   
Rnom = 1000      Area unit resistor =  $2\mu\text{m}^2$   
INLmean = 0.367036  
INLkmax\_mean = 0.000130823  
DNLmean = 0.46978  
INLtarget = 0.5000

Nruns = 100,000  
 Resistor Sigma = 14.1421  
INLsigma = 0.128294  
INLkmax\_sigma = 0.226276  
DNLsigma = 0.227768  
 Yield (%) = 84.8580

# Current Steering DACs



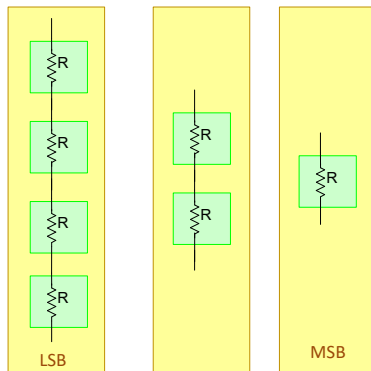
## Segmented Resistor Arrays

- Combines two types of architectures
- Can inherit advantages of both thermometer and binary approach
- Minimizes limitations of both thermometer and binary approach

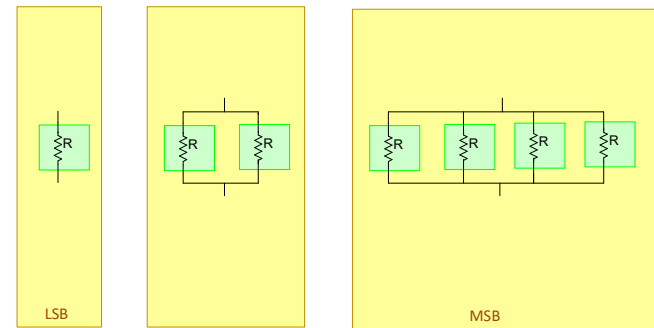
# Current Steering DACs

## Reduced Resistance Structure

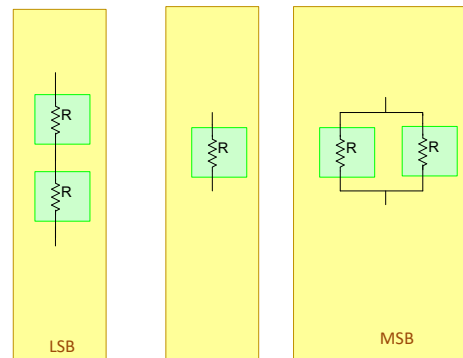
Is it better to use series unary cells to form  $R$  or parallel unary cells to form  $\frac{R}{2^n}$  ?



$2^n - 1$  cells



$2^n - 1$  cells



for n odd  $2^{\frac{n+3}{2}} - 3$  cells

n	Series	Parallel	Split
3	7	7	5
5	31	31	13
7	127	127	29
9	511	511	61
11	2047	2047	125
13	8191	8191	253
15	32767	32767	509

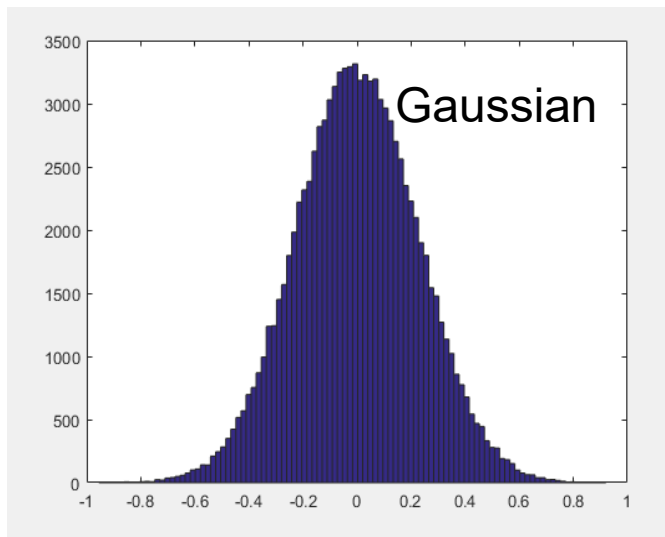
# Comparison of $INL_{kmax}$ and INL for String DACs

Example:  $n=10$

$A_R=0.02\mu m$   
 $R_N=1K$   
→

Resistor Sigma=  $14.14 \Omega$

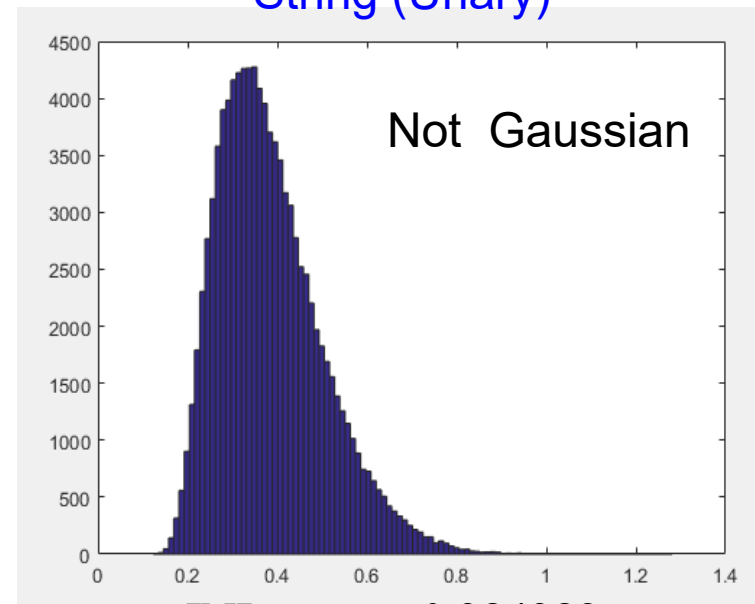
String (Unary)



$INL_{kmax\_mean} = -.00526008$

$INL_{kmax\_sigma} = 0.23196$

String (Unary)



$INL_{mean} = 0.384382$

$INL_{sigma} = 0.117732$

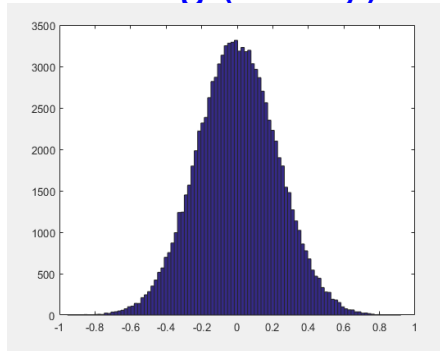
- Closed-Form Analytical Formulation Available
- No Closed-Form Analytical Formulation

Histogram of INL from 100,000 runs

File: BinaryWeightedDACInl.m

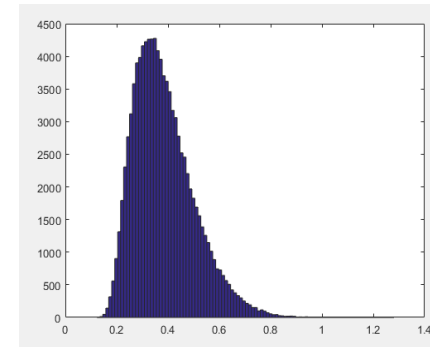
# Comparison of INL and $INL_{kmax}$

String (Unary)

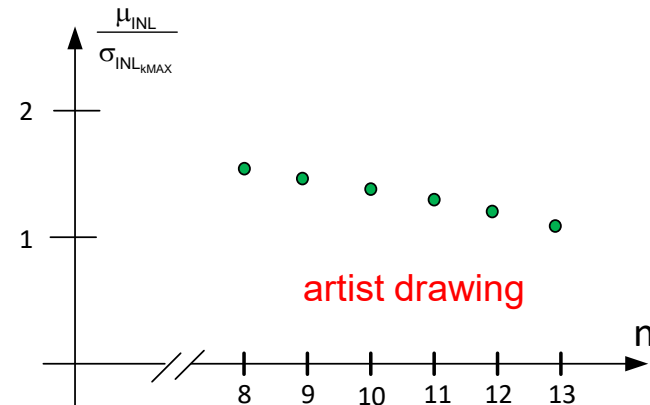
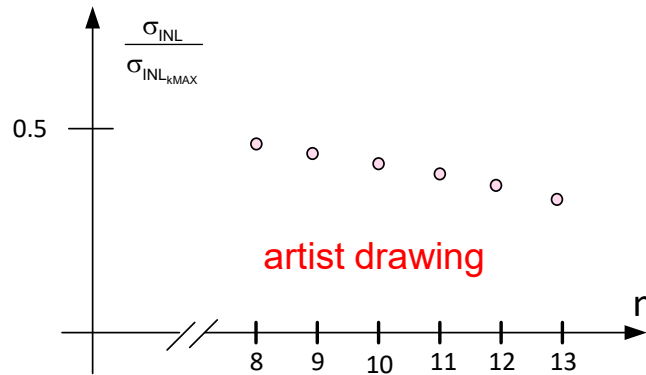


Histogram of  $INL_{kmax}$

String (Unary)



Histogram of INL



These plots may be useful for providing insight into performance

Results similar for both String and Binary Structures

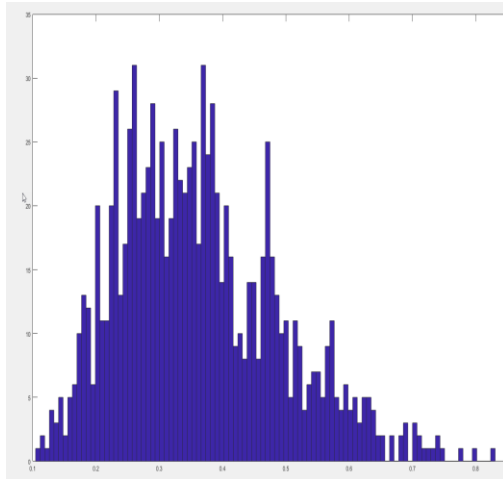
# Monte Carlo Simulation Time can Become Large

Example:  $n=10$

$A_R=0.02\mu\text{m}$   
 $R_N=1\text{K}$   
→

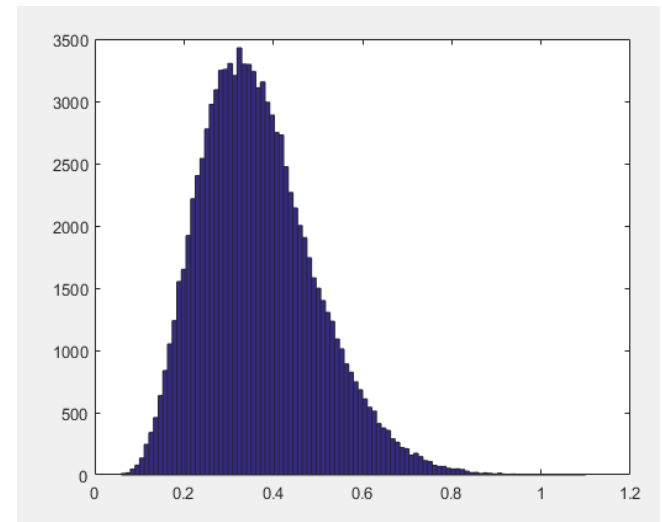
Resistor Sigma=  $14.14\ \Omega$

Binary DAC



Histogram of INL from 1000 runs

Binary DAC



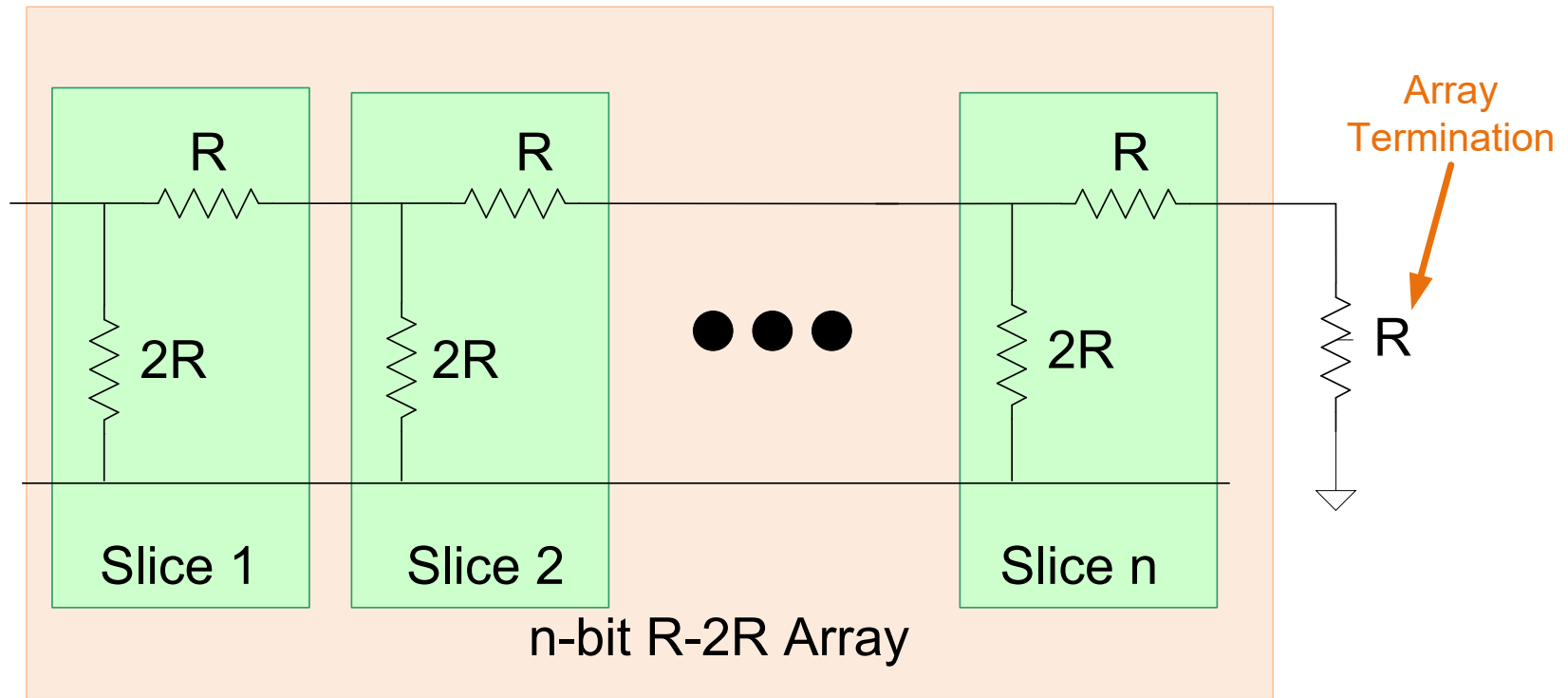
Histogram of INL from 100,000 runs

Can require a large number of runs for useful information

This should provide insight into length of Monte Carlo simulations needed to get useful results

# The R-2R Ladder

# R-2R Resistor Arrays



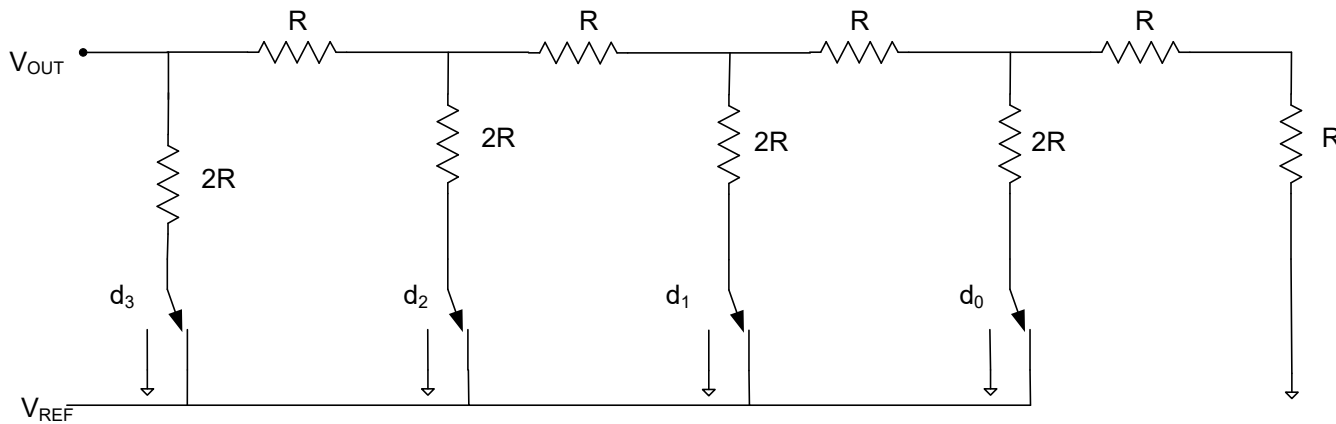
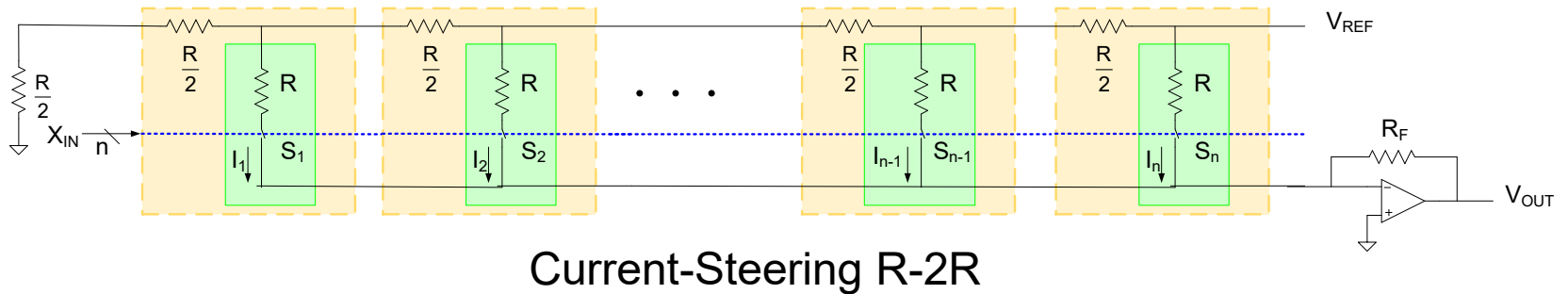
- Conceptually, area goes up linearly with number of bit slices
- Can be used in many different ways



# R-2R DAC



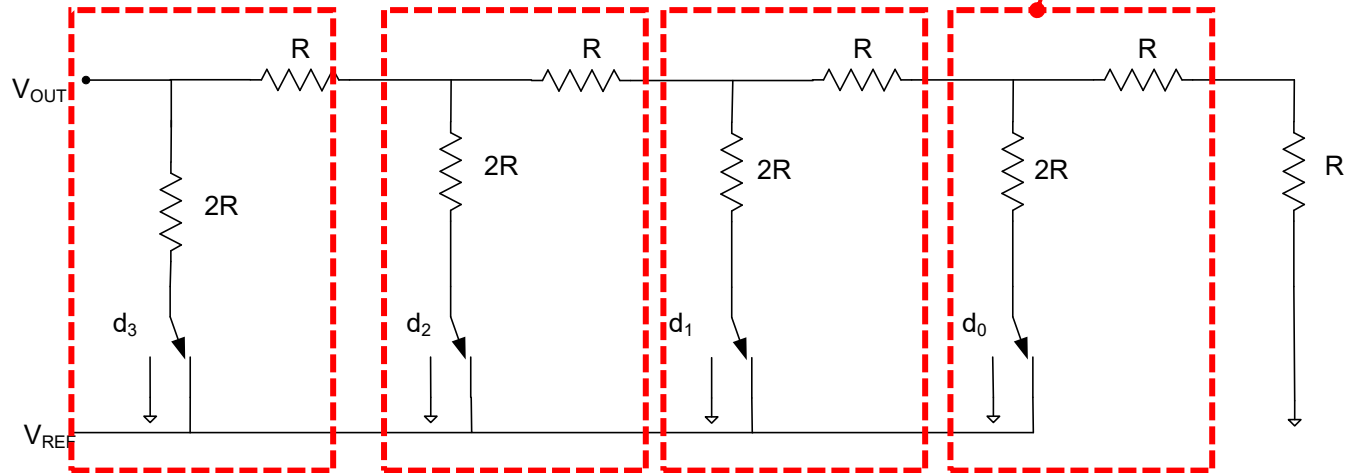
## Various Implementations of the R-2R Structure



# R-2R DAC



Voltage-Division Structure (4-bits shown)



By superposition:

$$V_{OUT} = V_{REF} d_3 \cdot \frac{1}{2} + V_{REF} d_2 \cdot \frac{1}{4} + V_{REF} d_1 \cdot \frac{1}{8} + V_{REF} d_0 \cdot \frac{1}{16} = V_{REF} \sum_{k=0}^3 \frac{d_k}{2^{4-k}} = V_{REF} \sum_{k=1}^4 \frac{d_{4-k}}{2^k}$$

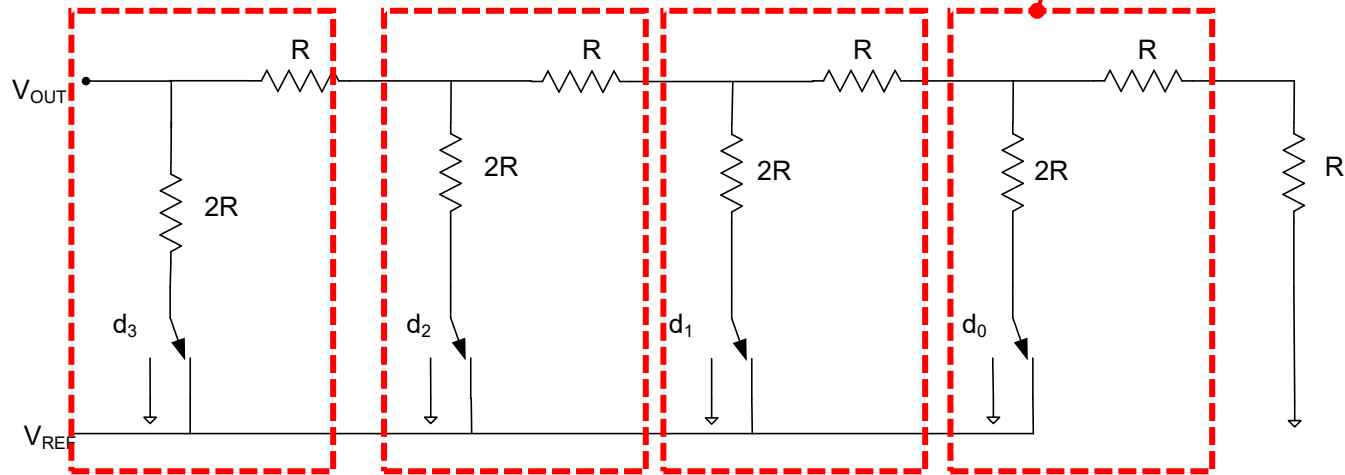
- No op amp required !!
- 2:1 Ratio matching of MSB slice most critical
- Total resistance goes up linearly with number of bit slices !!
- Conventional wisdom: area goes up linearly with number of bit slices
- Does conventional wisdom result in optimal designs?

# R-2R DAC



Voltage-Division Structure

(4-bits shown)

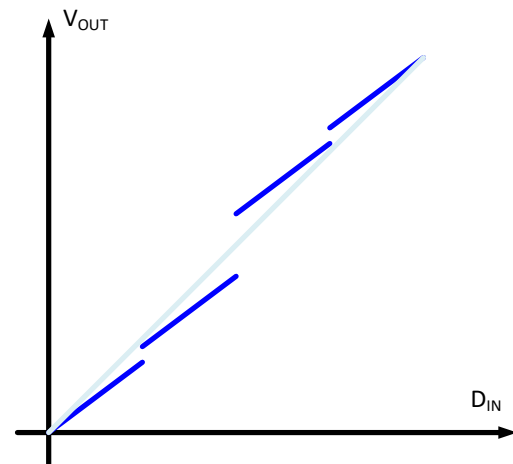
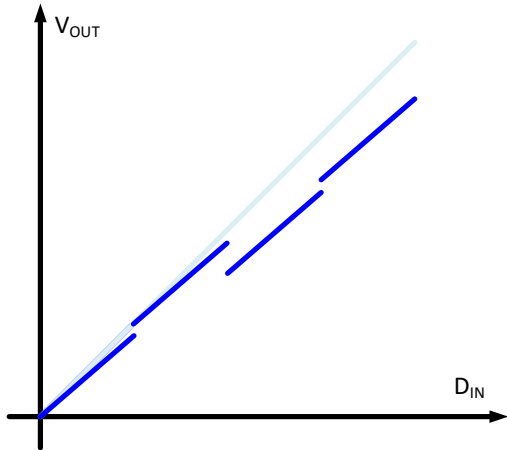
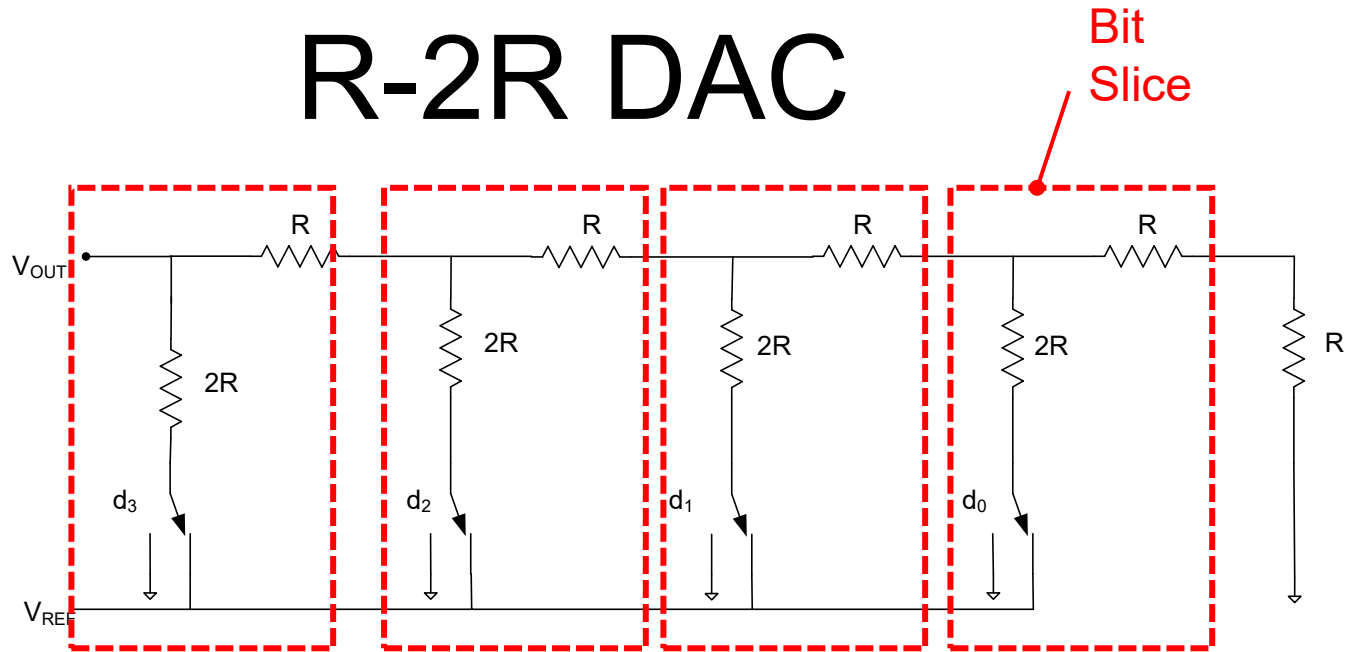


Limitations:

- Parasitic capacitances on all nodes must settle during all transitions
- Switch impedances imbalance  $2R$  cells
- Analogous to top-plate switching
- Output impedance not 0

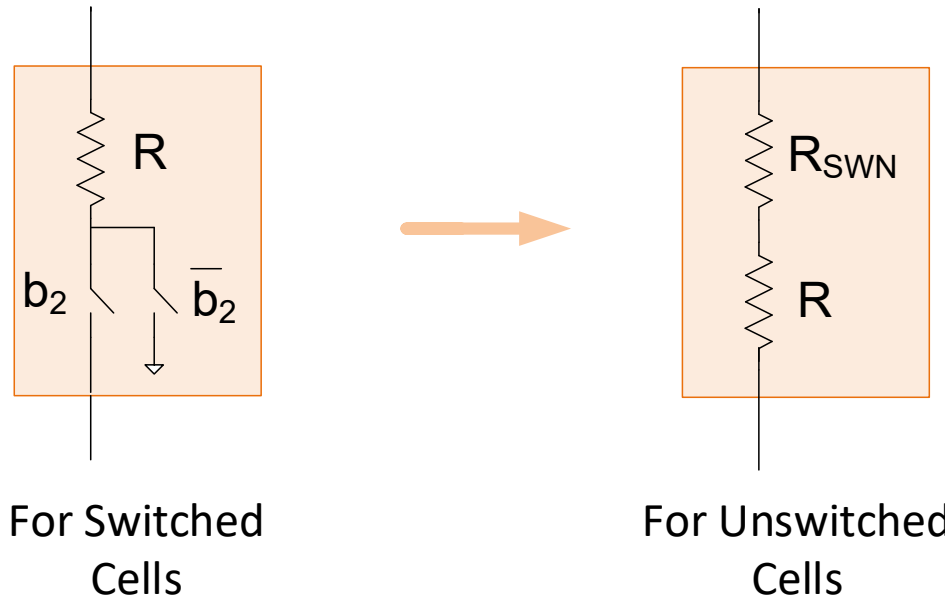
Is the output impedance code dependent?

# R-2R DAC



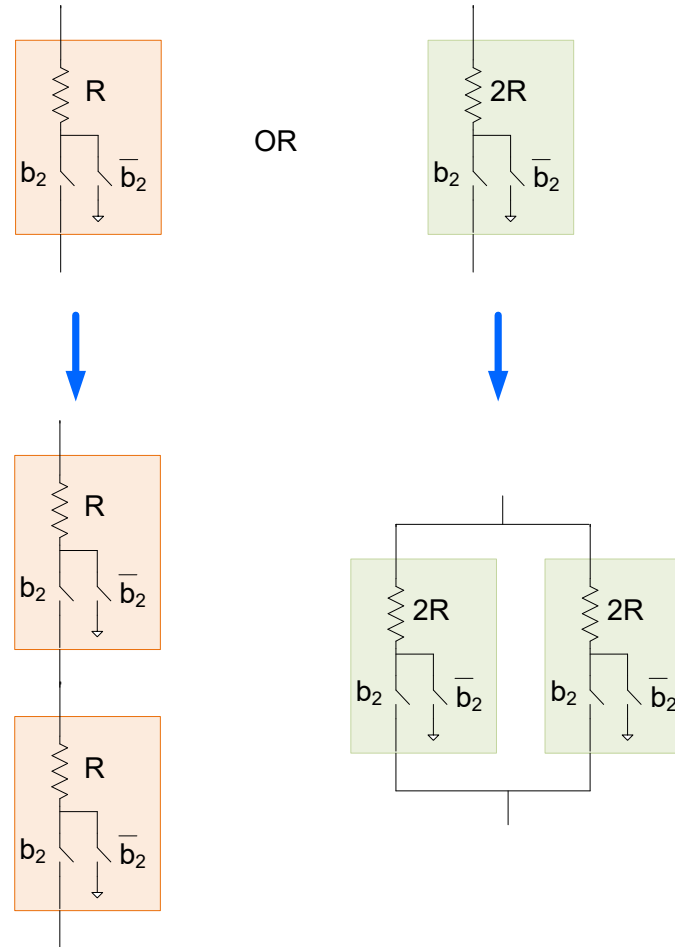
Large steps in output can occur  
How should area be allocated?

# R-2R Implementation



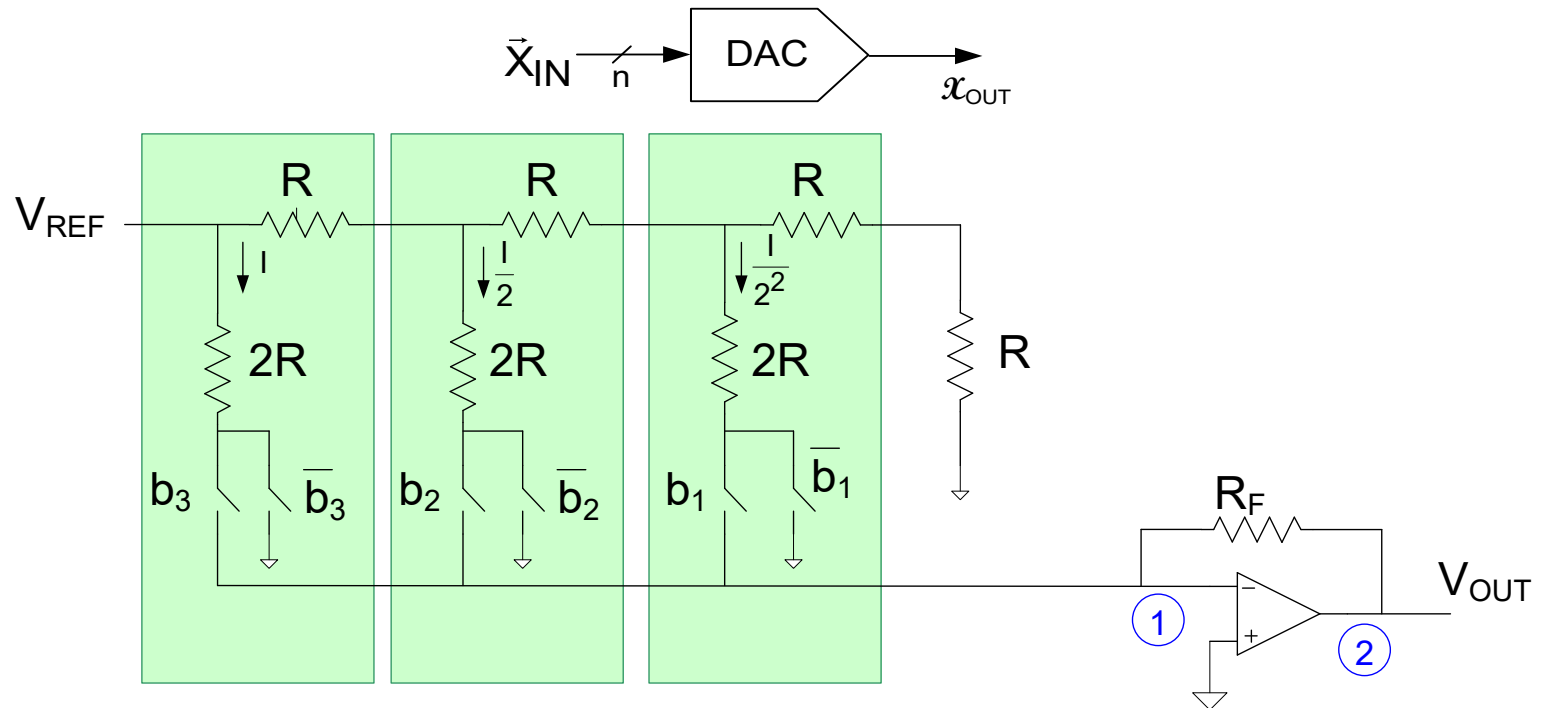
- Add resistor equal to nominal switch impedance in each unswitched cell
- Impedance equal to the nominal switch impedance
- Offers some improvement, particularly if all switches are bottom-plate switches  
(but for previous R-2R structure do not have all bottom-plate switches)
- Will not track with temperature and process variations

# R-2R Implementation



- Unit cell widely used
- Switch included in cell even if not switched!
- Code dependence of switch impedance of concern (this can be addressed)
- Delays associated with turning on switches also of concern since some cells not referenced to same level as switches

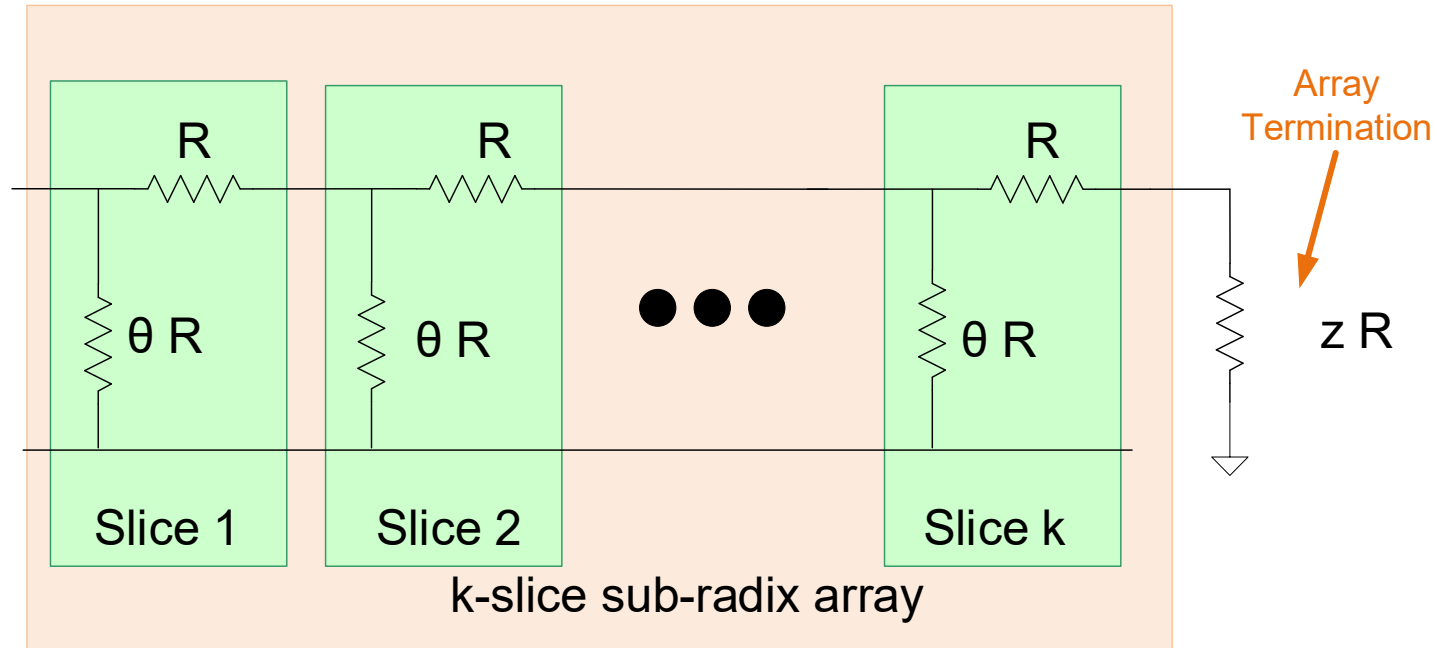
# R-2R Current Steering DAC



- INL can get large in R-2R structures
- DNL can get large in R-2R structures

# Sub-radix Array

Want Currents to Scale by  $1/\theta$  (instead of  $1/2$ ) from each slice to the next



Typically  $2.1 < \theta < 2.5$

Termination resistor must be selected so that same attenuation is maintained

Often only the first  $n_1$  MSB “slices” will be sub-radix

Effective number of bits when using sub-radix array will be less than  $k$

Can be calibrated to obtain very low DNL (and maybe INL) with small area



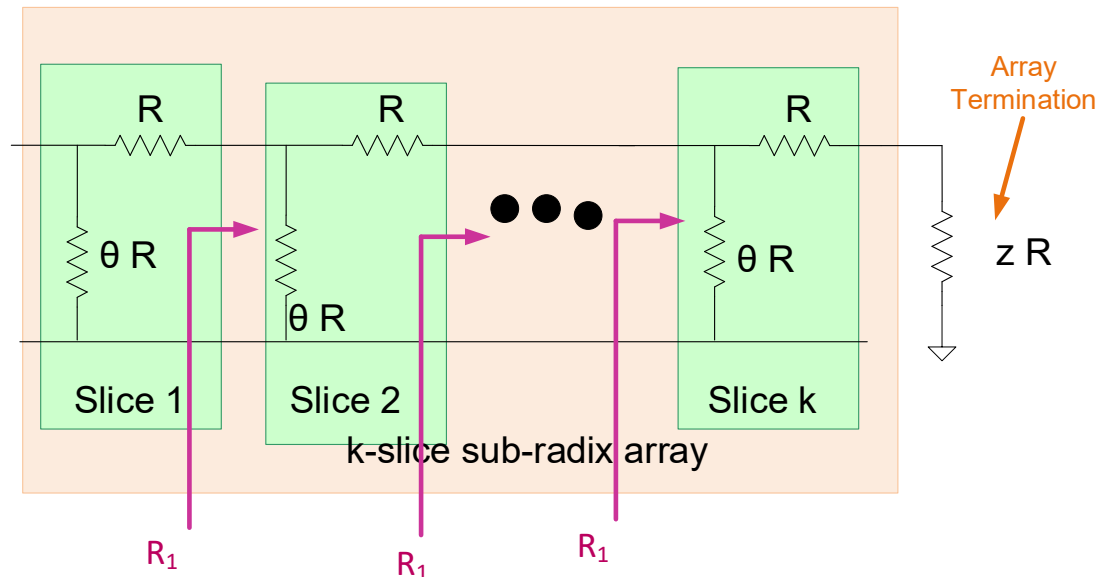
# Sub-radix Array

It can be shown that the optimal value of  $z$  is given by the expression

$$z = \frac{3\theta + 1 - (1 + \theta)\sqrt{1 + 4\theta}}{-1 + \sqrt{1 + 4\theta} - 2\theta}$$

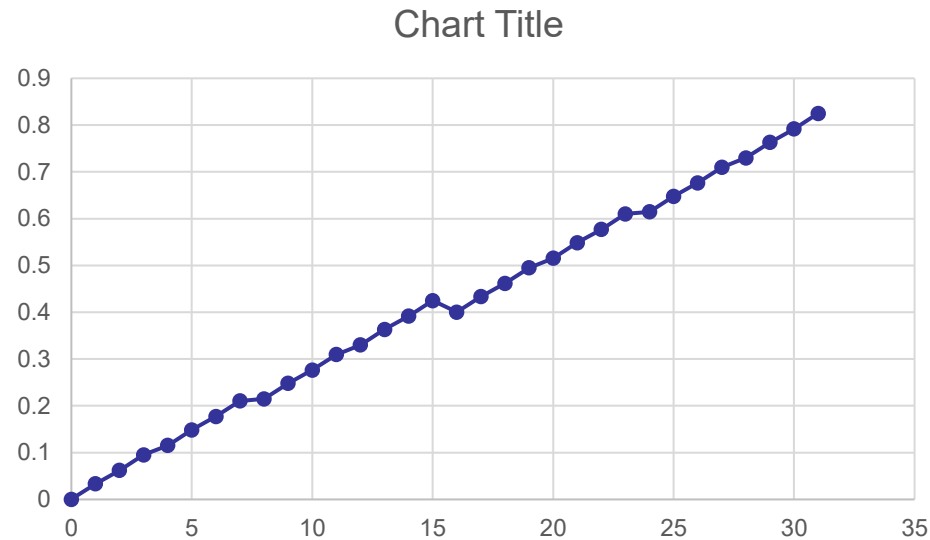
This derivation is in a file named Termination of Subradix.docx

Derivation based upon assuming the three impedances  $R_1$  below must be the same



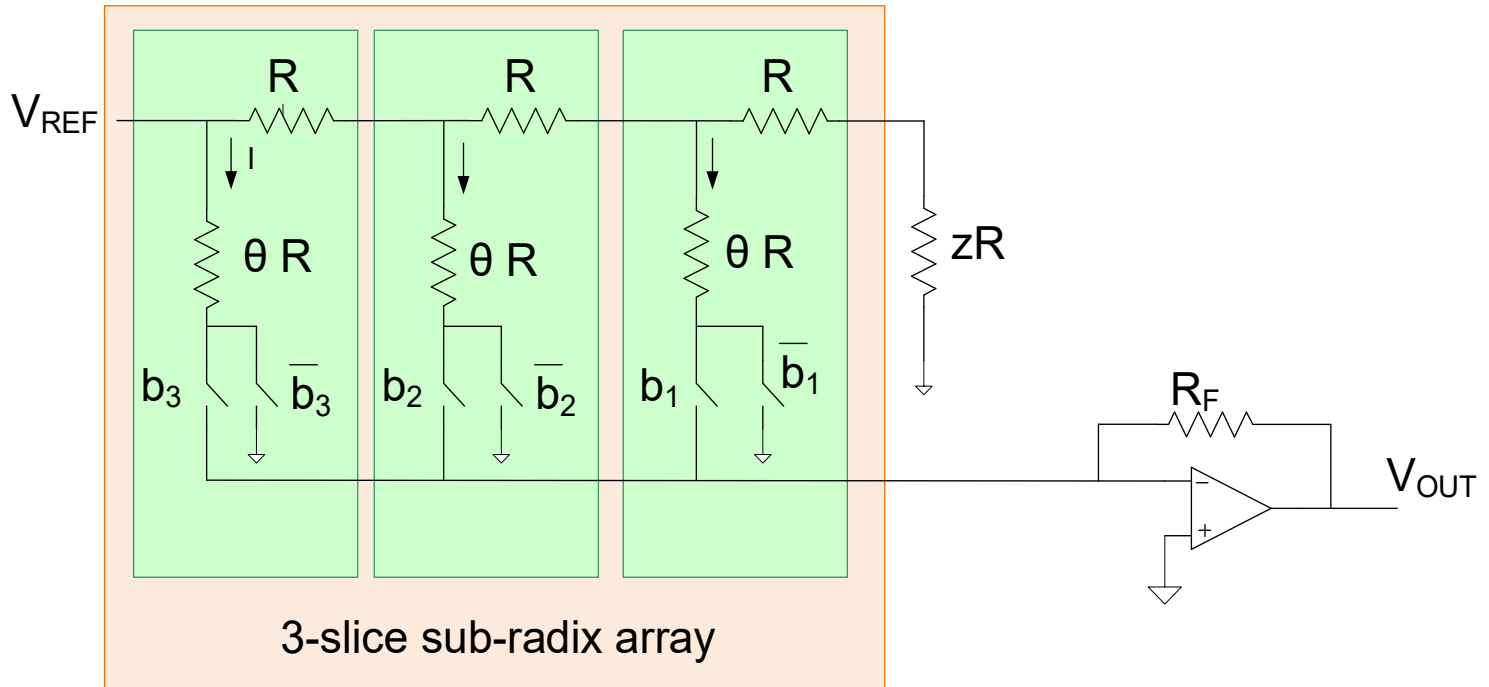
Output of an optimally terminated subradix DAC of 5 bits with  $\theta=2.5$  and  $z=1.15831$

See file SubRadix DAC.xlsx



$\theta$  selected so probability of large positive gap is very small

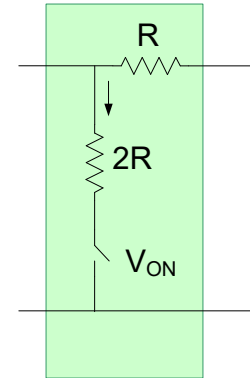
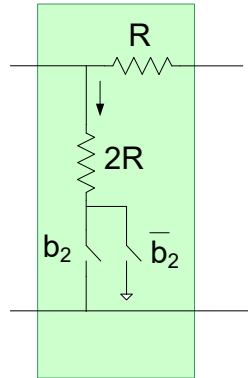
# 3-slice sub-radix DAC



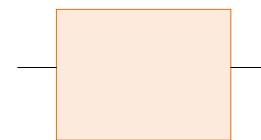
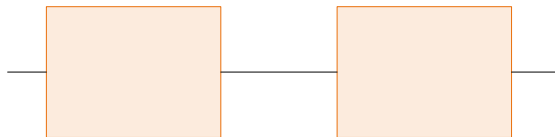
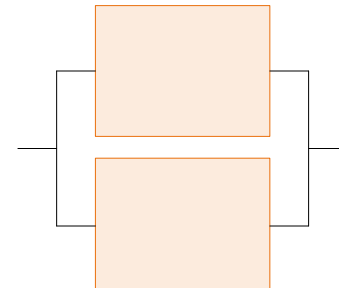
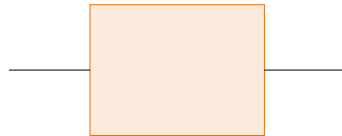
Typically  $\theta$  is slightly greater than 2

Does not eliminate large DNL errors but can eliminate gaps in output

# R-2R Resistor Arrays



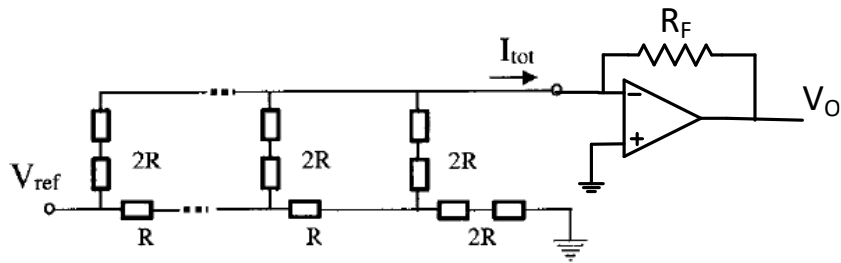
Does it make any difference how area is allocated?



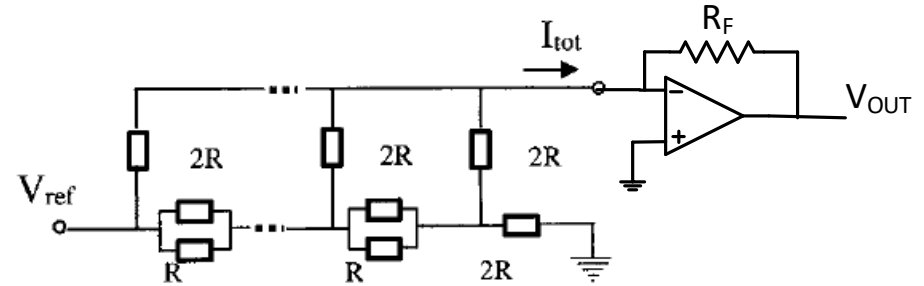
2R Area twice R Area

R Area twice 2R Area

# Area Allocation for R and 2R Resistors

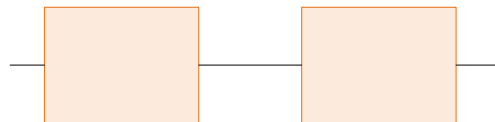


Switches not shown



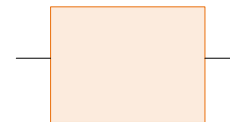
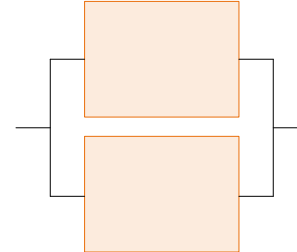
Switches not shown

Series Layout



2R Area twice R Area

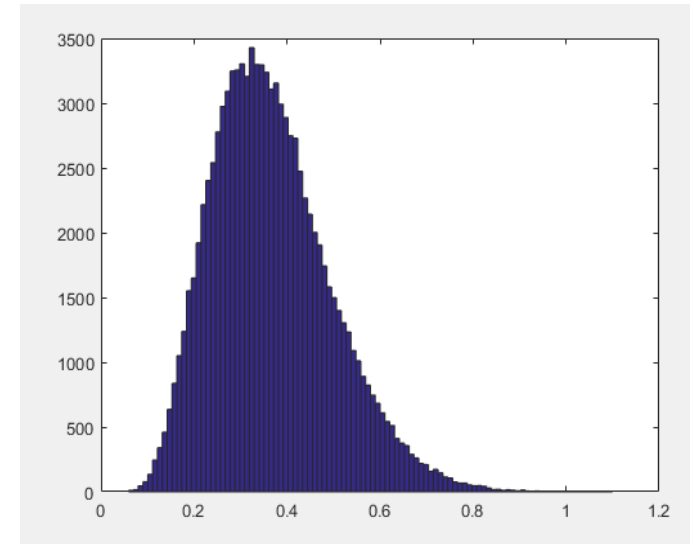
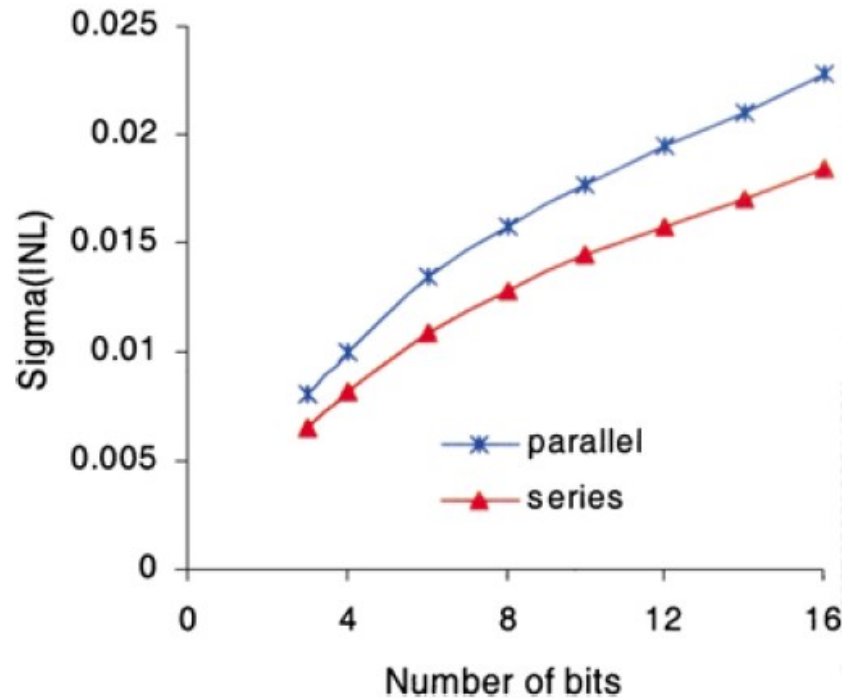
Parallel Layout



R Area twice 2R Area

Assume area in each slice if fixed

# Area Allocation for R and 2R Resistors

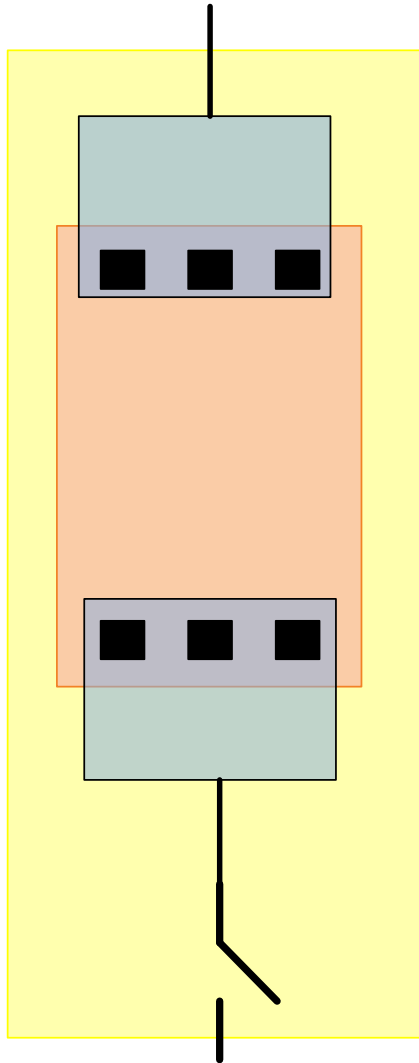


Yield is affected by both mean and standard deviation of the non-Gaussian pdf

Standard deviation of parallel layout is somewhat more (but uses less cells for n small)

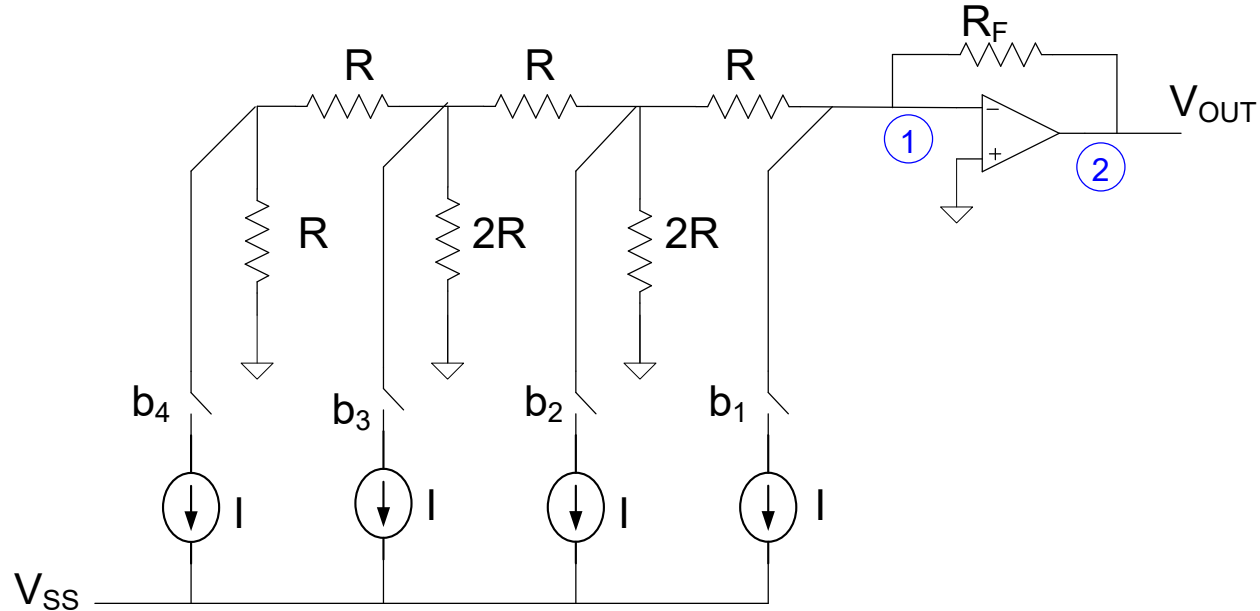
Area allocation between slices also affects yield

# Challenges with all R-based DACs



- Switch Impedance
- Contact Resistance
- Variability
  - Resistor
  - Contact Resistance
  - Switch Impedance
- Parasitic Capacitances

# Another R-2R DAC



Eliminates series switch resistance when switching resistors

Series resistance in current source does not affect current

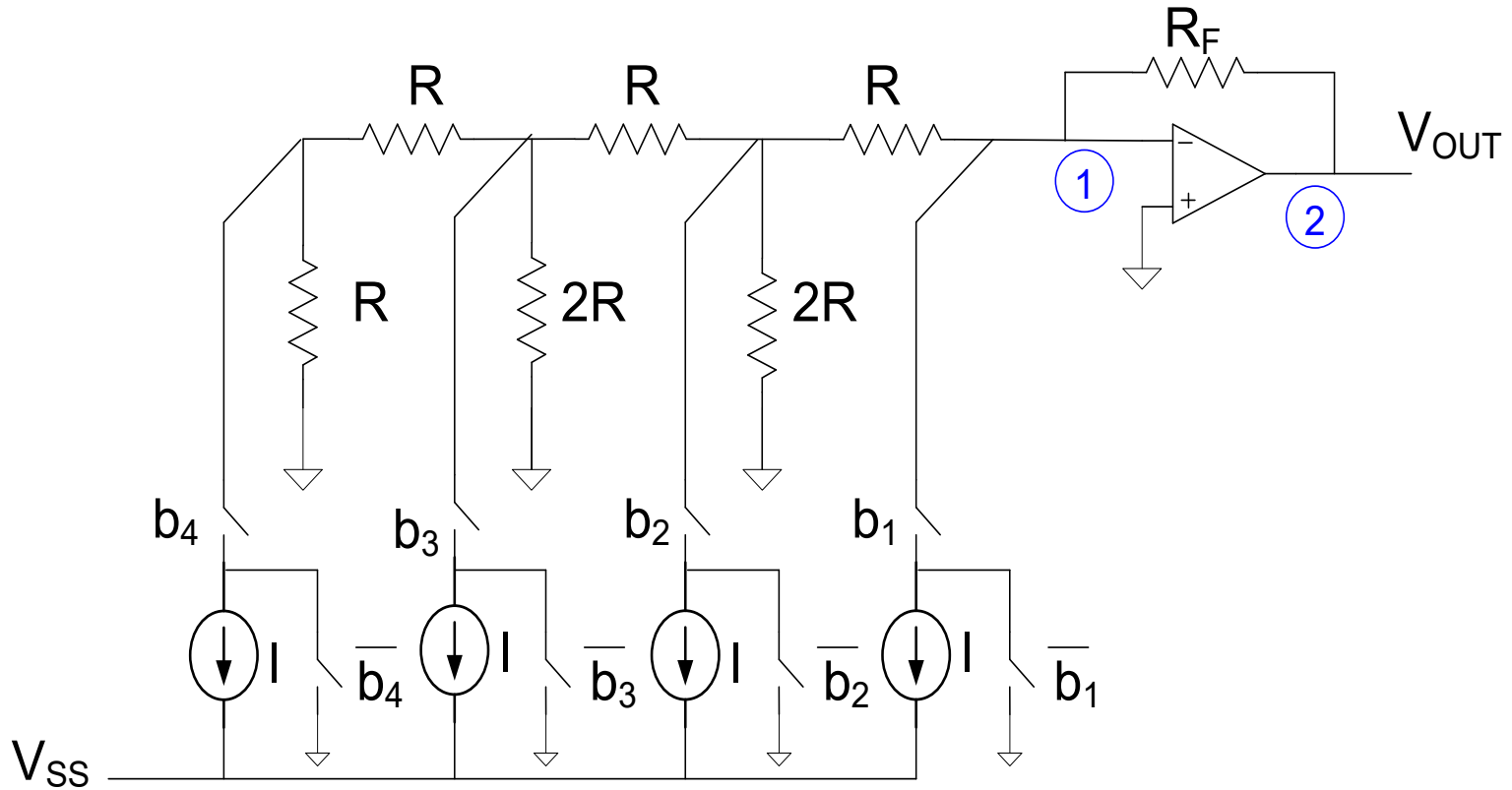
Must match both resistors and current sources

Current flow will pull capacitance on switch nodes to low before current sources leave saturation

Current flow will change power dissipation based upon digital code



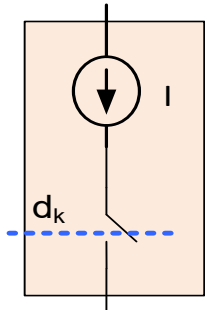
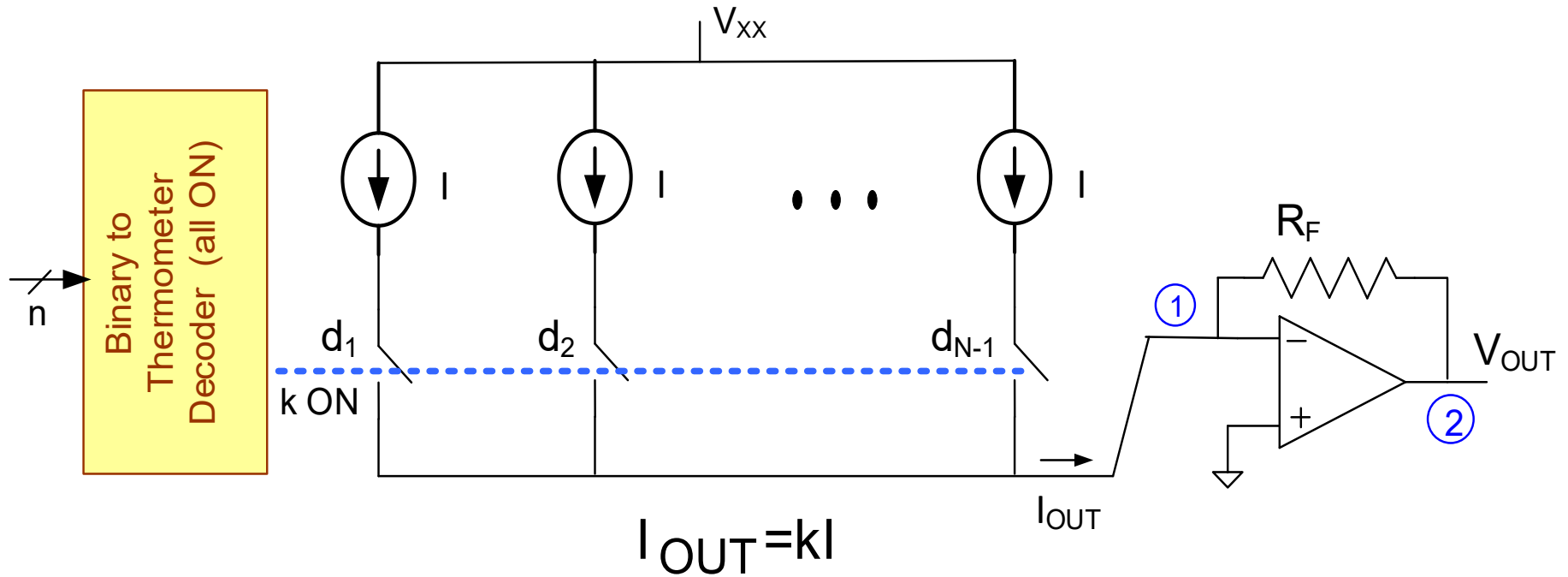
# Another R-2R DAC



Switch will pull capacitance on switch nodes to GND instead of  $V_{SS}$

Power dissipation will not be code dependent

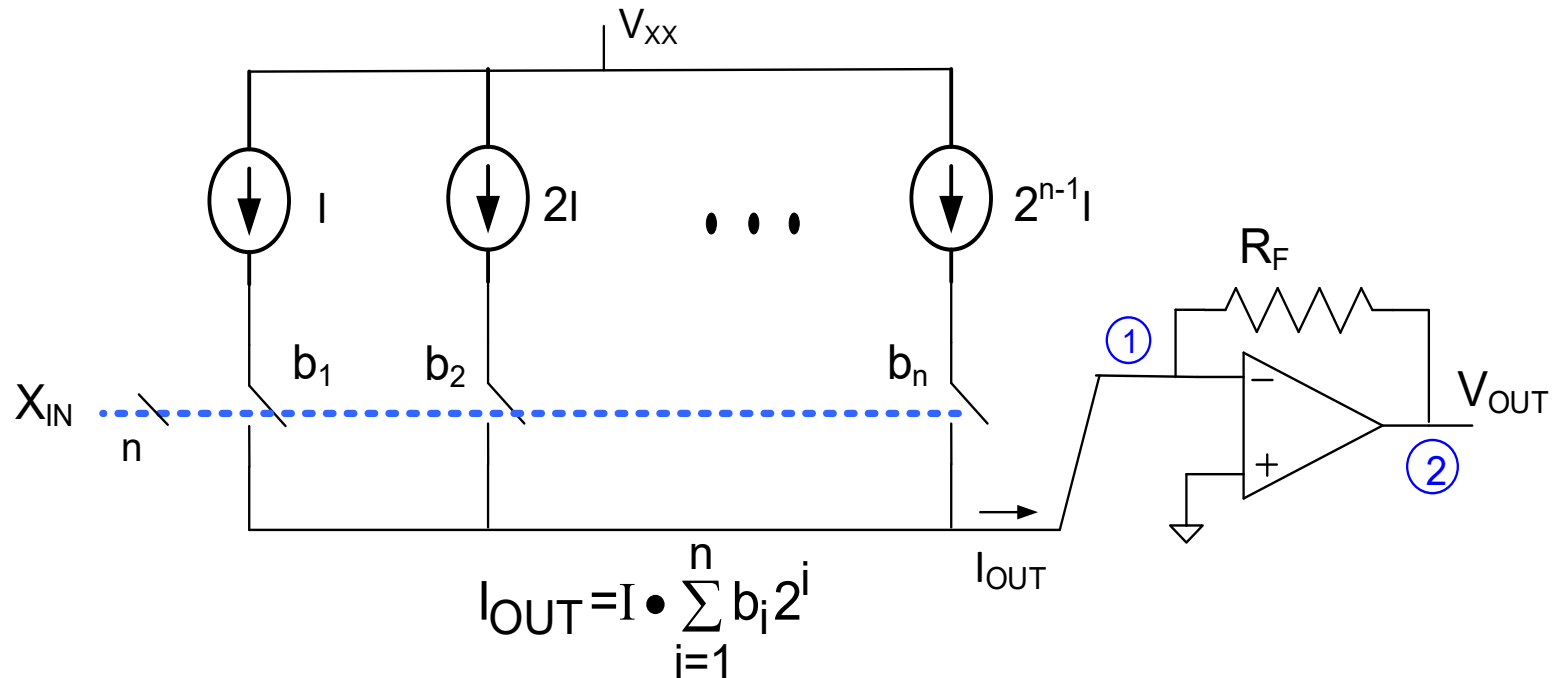
# Current Steering DAC



Unary Slice Cell

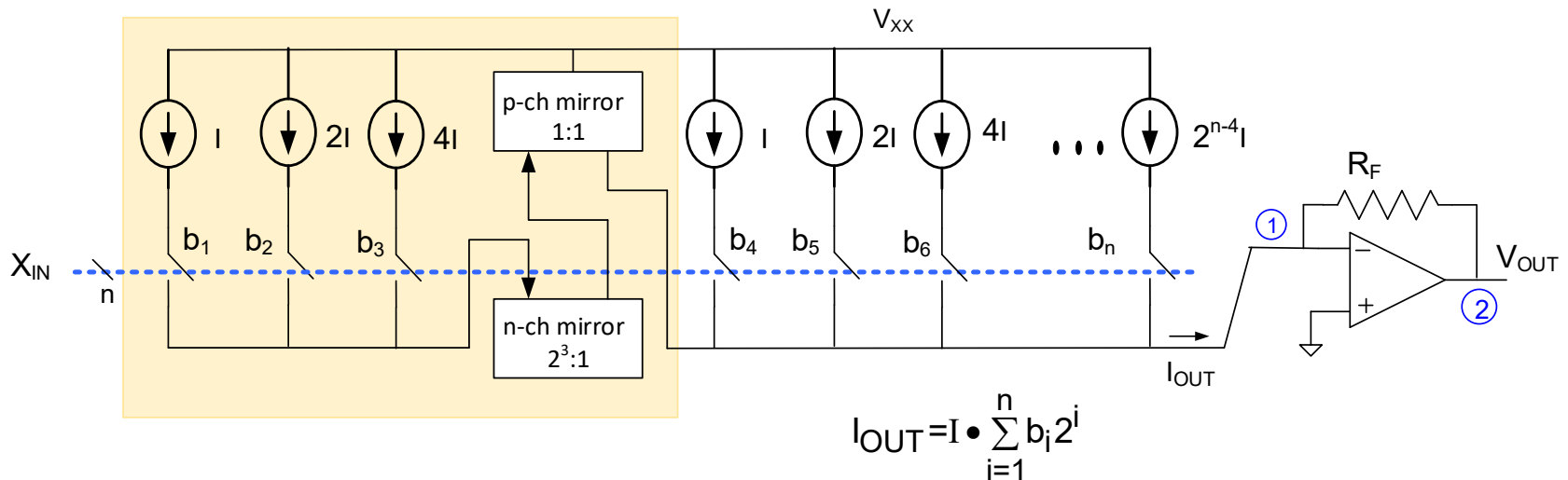
- Switch impedance of little concern
- Bottom-plate switching
- Low DNL
- Decoder impractical for large  $n$

# Current Steering Binary DAC



- eliminates decoder
- DNL not good for large  $n$
- area ratio from MSB source to LSB source too large for large  $n$  (can make  $I$  only so small)

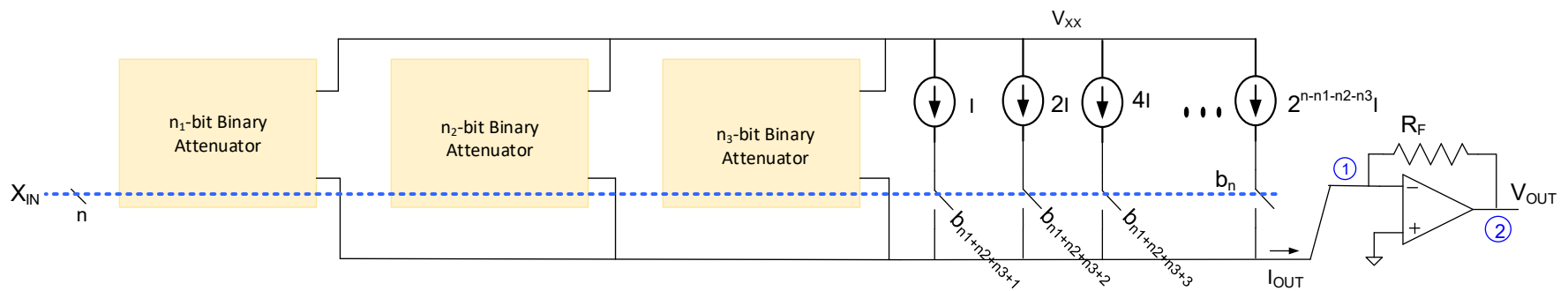
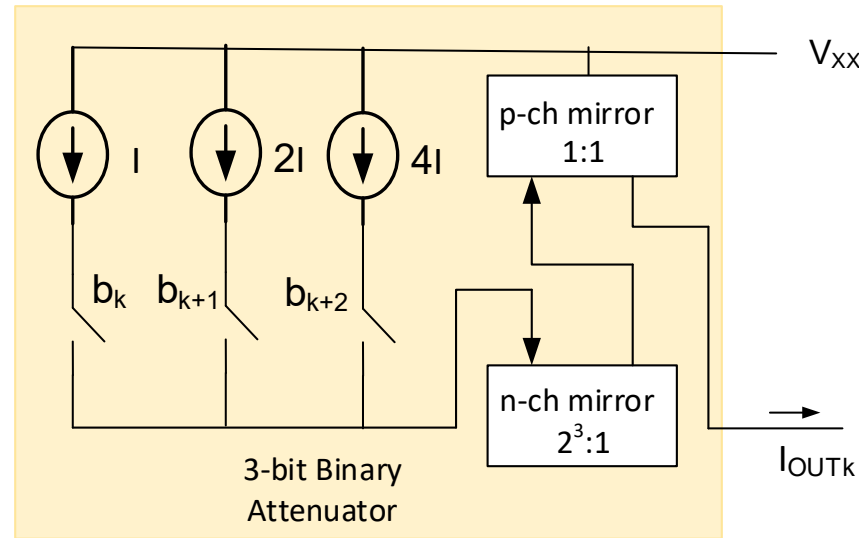
# Current Steering Binary DAC



- reduces total current spread of bit cells
- reduces total number of bit cells (since cells are bundled)
- can repeat mirror current attenuator
- can change number of bits in each current attenuator stage
- Scale currents down in LSB portion rather than scale current up in MSB portion

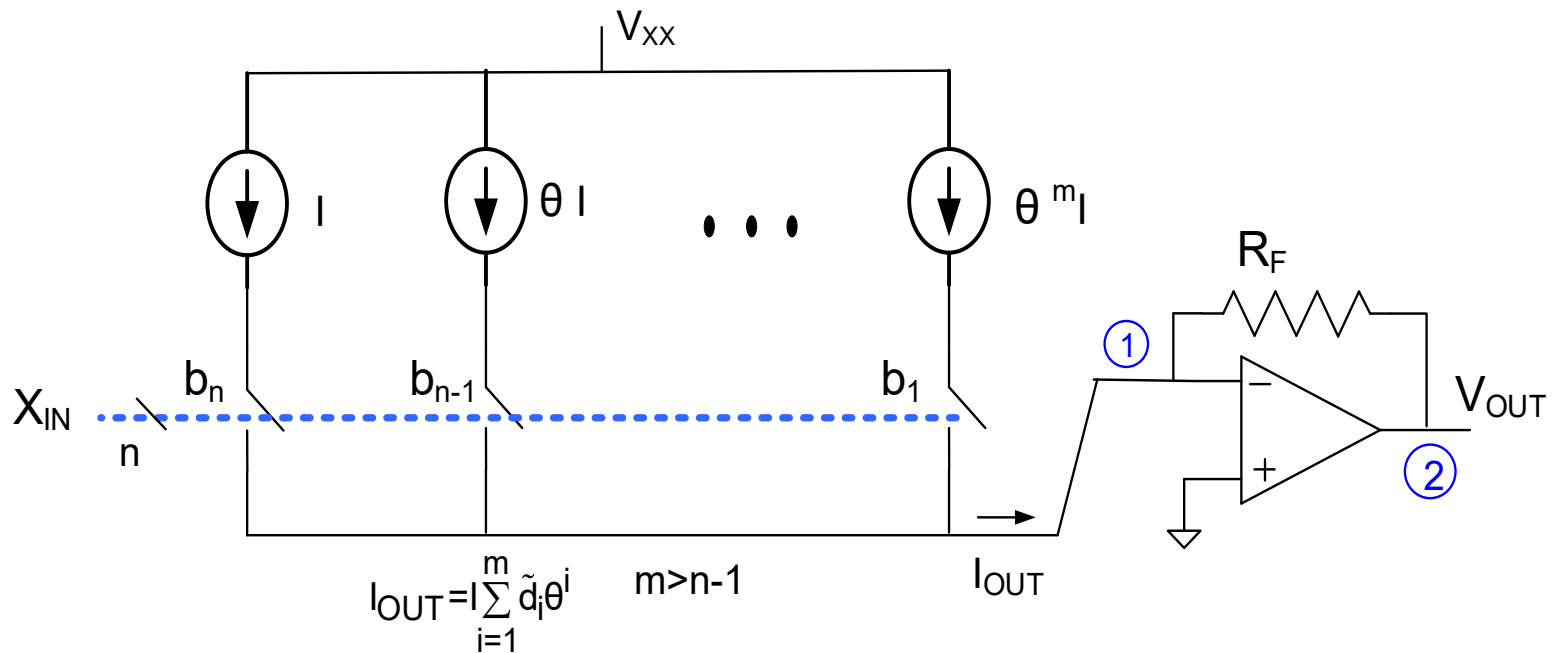
How is performance affected by reducing the number of unary cells?  
Is too much area allocated to the LSB cells?

# Current Steering Binary DAC



- LSB performance not critical
- Limit number of binary attenuators to avoid accumulating too much error

# Sub-Radix Current Steering DAC

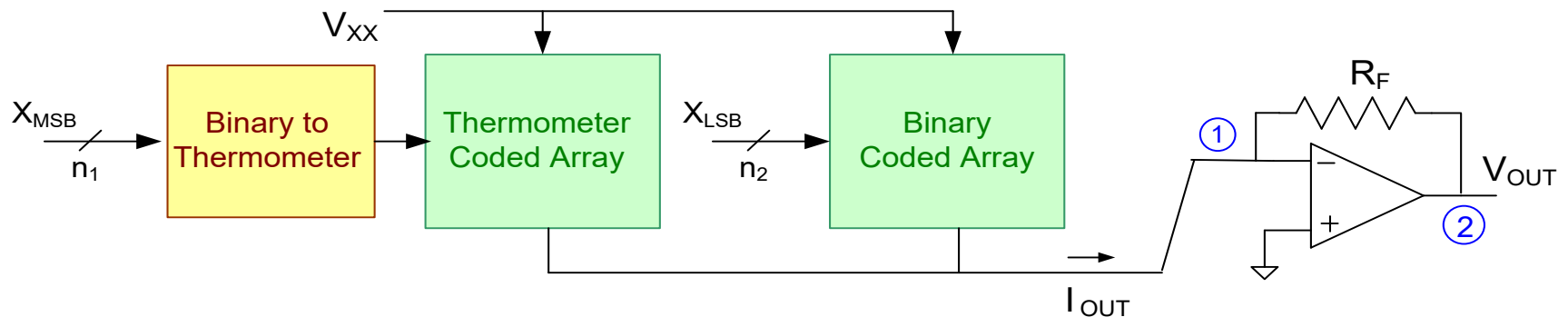


Typically  $1.9 < \theta < 1.99$  (Depending on ratio-matching accuracy of current sources)

Takes smaller steps so takes more steps to cover range

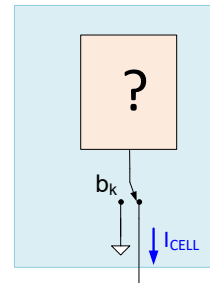
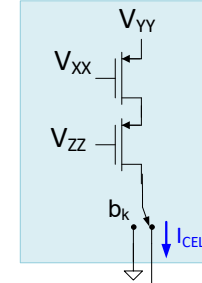
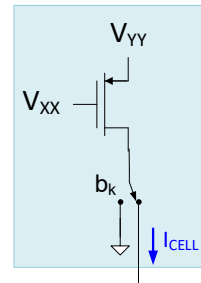
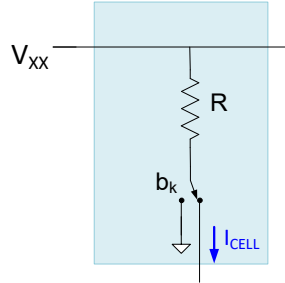
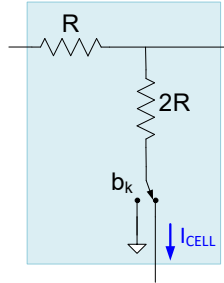
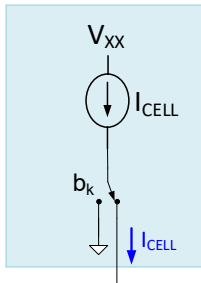
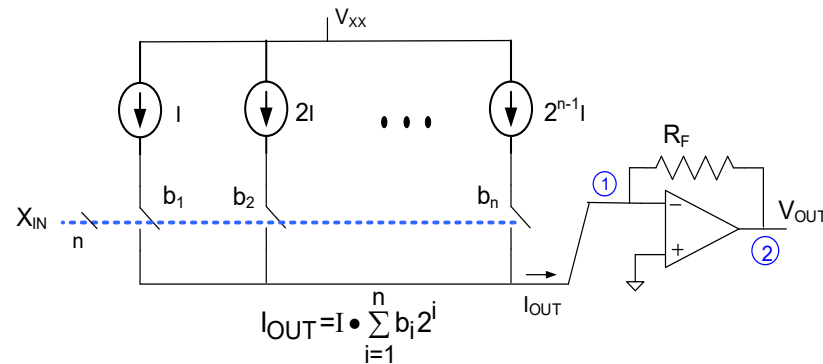
# Current Steering DAC

## Segmented Structure Widely Used



- Binary code LSBs to reduce Decoder Complexity
- Thermometer Code MSB to manage DNL
- Partitioning between Thermometer and Binary Coding is critical

# What Cells Are Used for Current Steering DAC



- What characteristics are important in a given process ?

$R_{OUT}$ ?

Speed?

Matching?

Power ?

Area (cost) ?

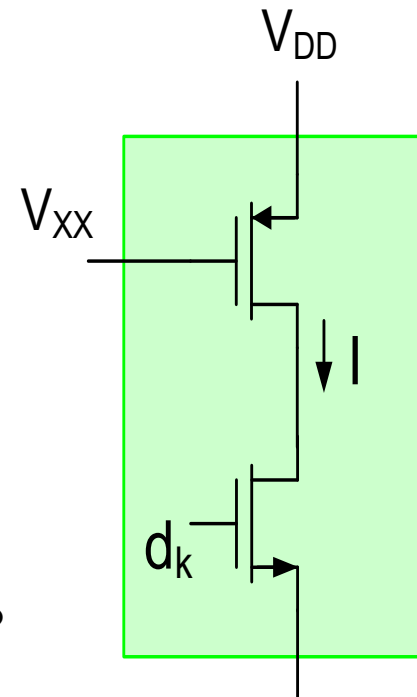
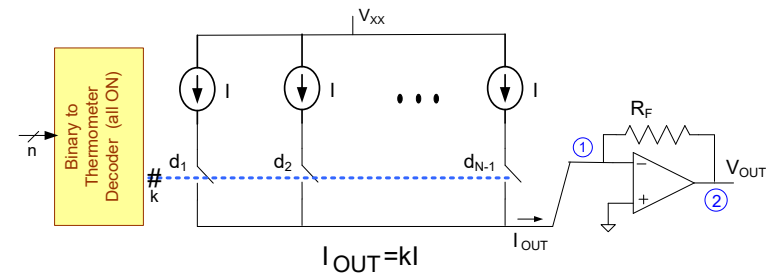
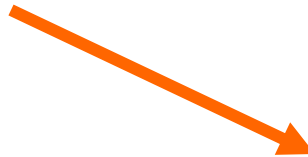
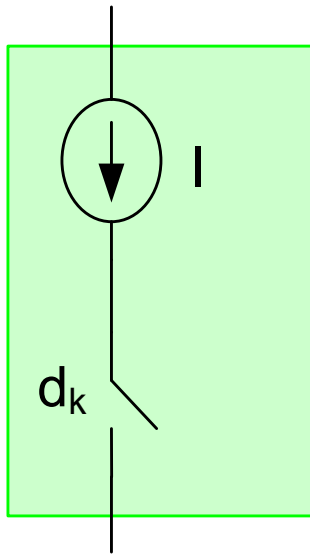
Linearity ?

- What cells are used ?



# Current Steering DAC

## Current Source Bit Cells:



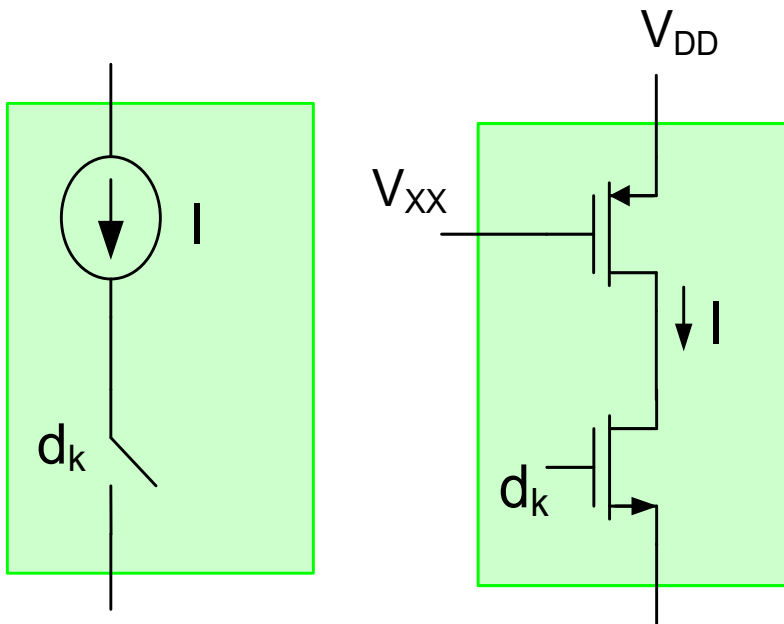
Bottom plate switching

Is output impedance of current sources of concern?

No ! Matching is important but linearity is not

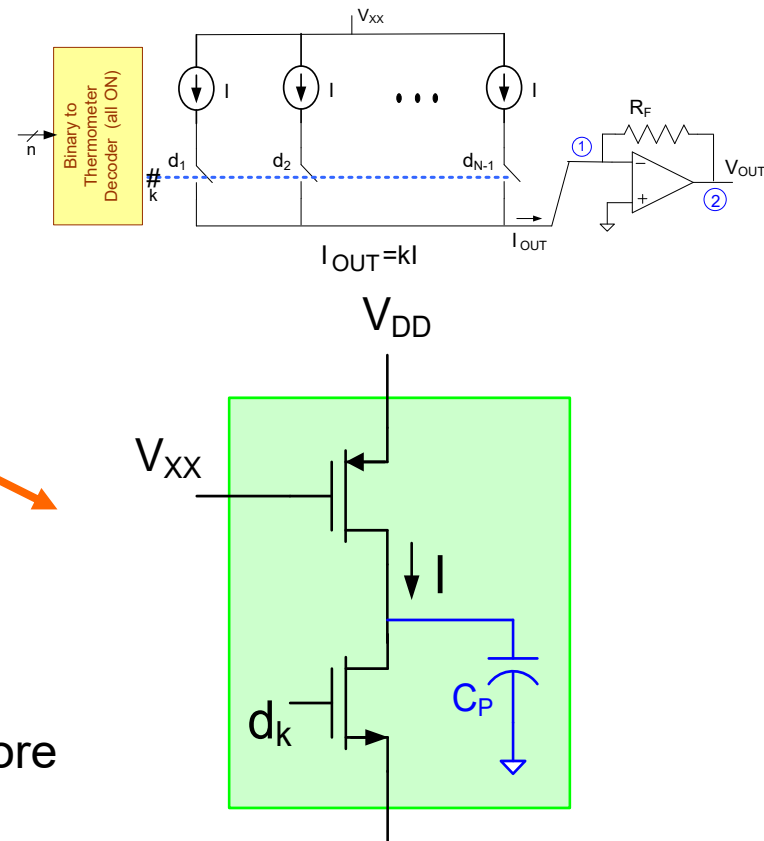
# Current Steering DAC

## Current Source Bit Cells:

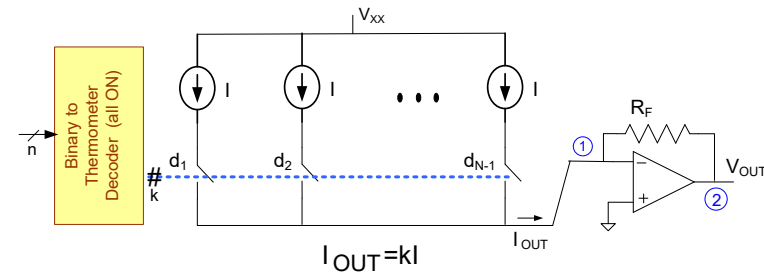
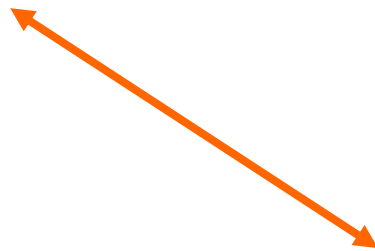
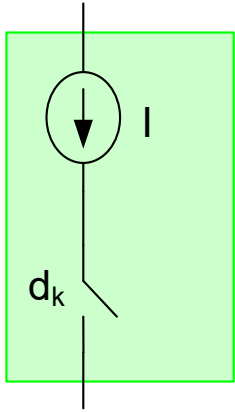


Parasitic capacitance will charge to  $V_{XX}$  before current source saturates

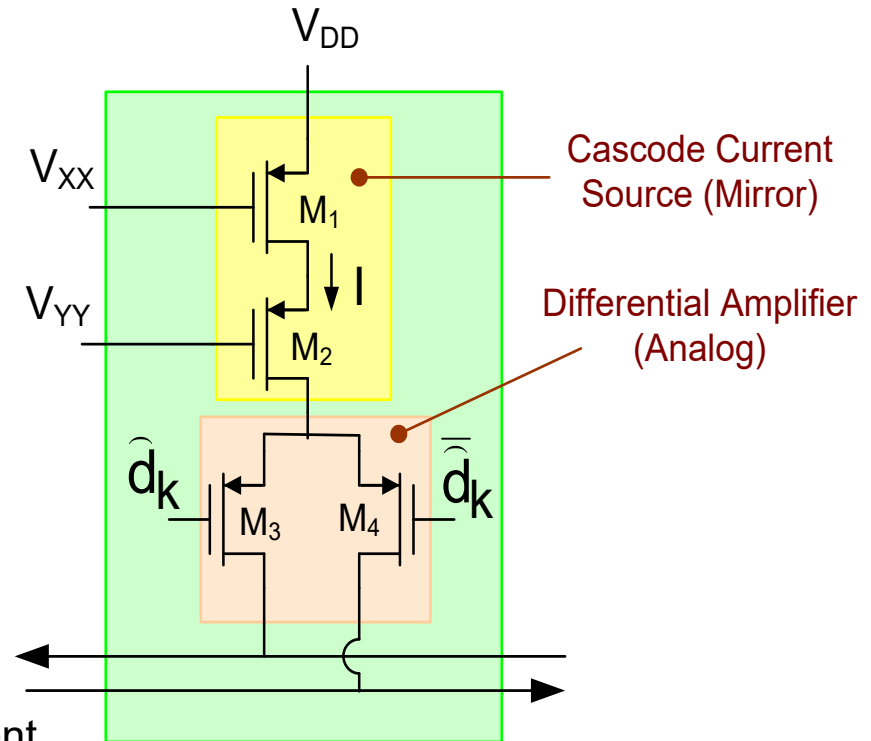
Power dissipation is code dependent



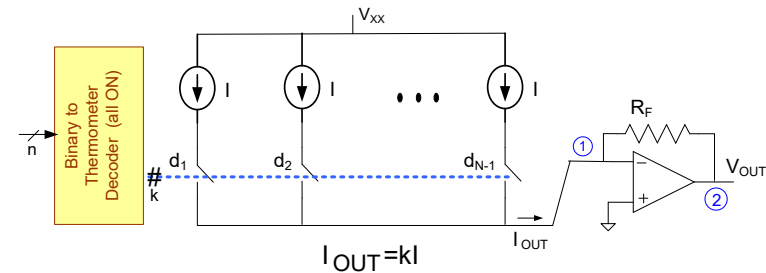
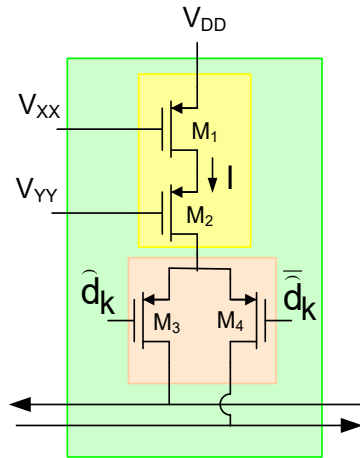
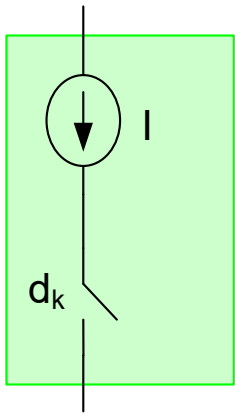
# Current Steering DAC



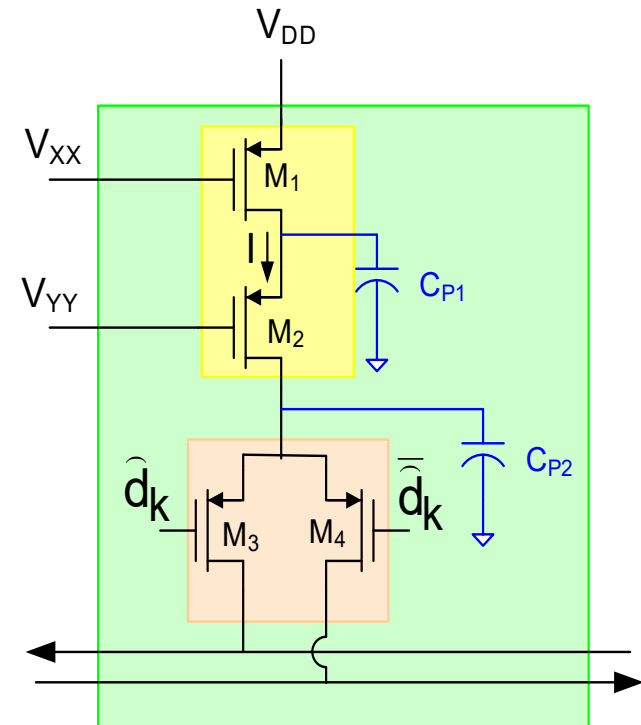
- Current steering instead of current switching
- Power dissipation in current sources remains constant
- Smaller gate voltages can be used to steer current
- Dump current can provide differential DAC output



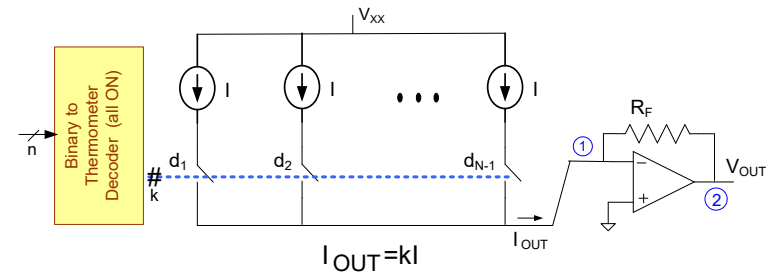
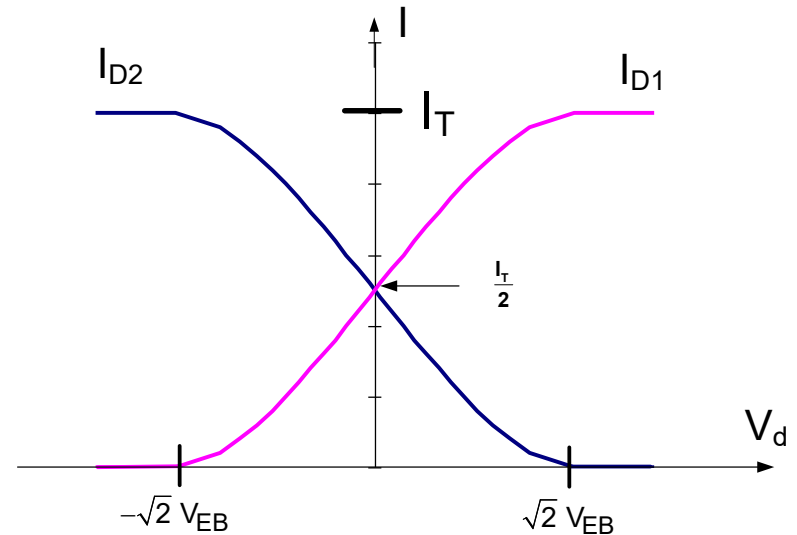
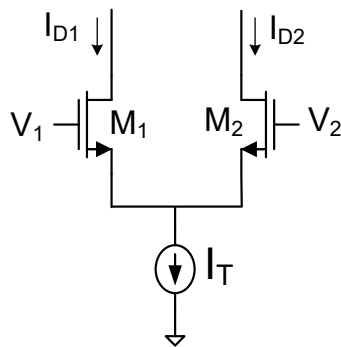
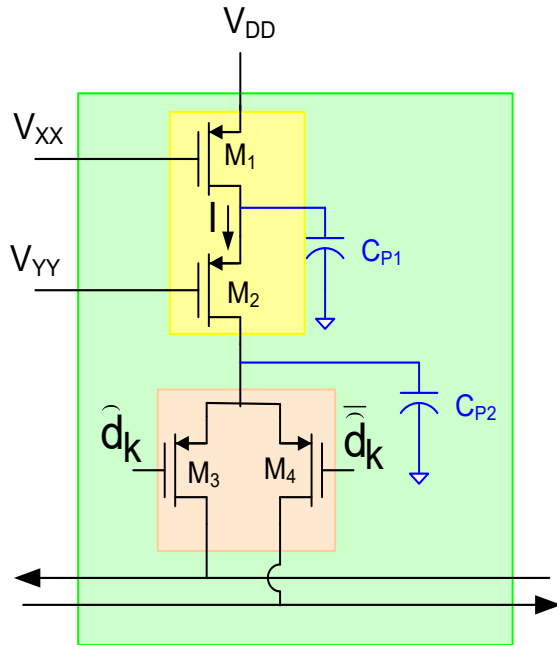
# Current Steering DAC



- Parasitic capacitances do not charge and discharge
- Current steering provides inherent cascading
- This structure is a double-cascode

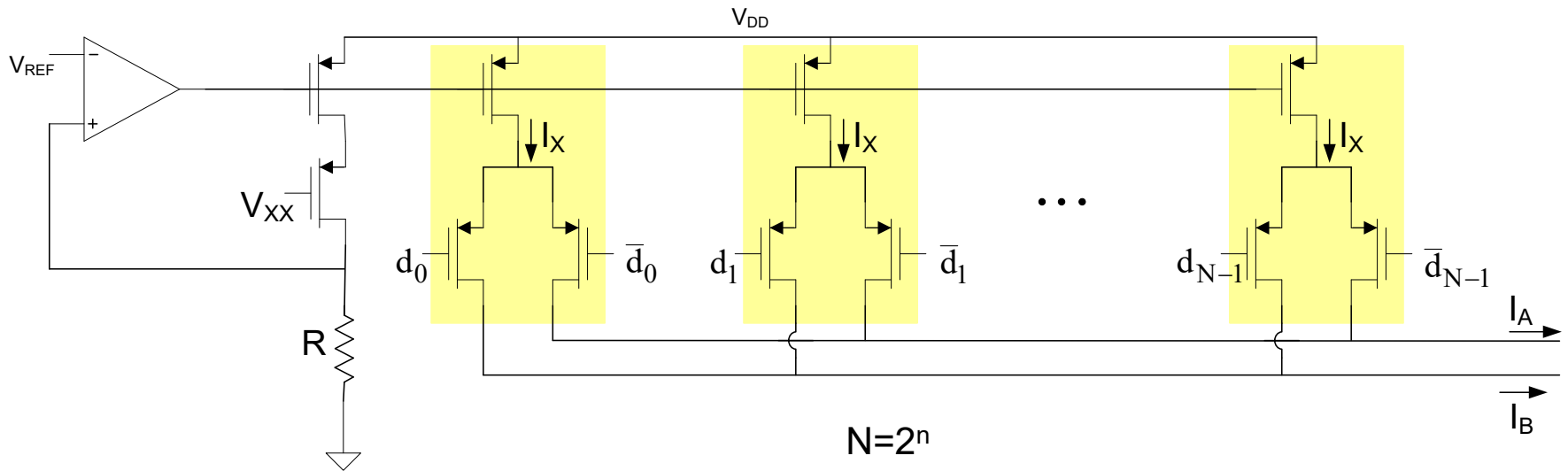


# Current Steering DAC



Signal swings only need to be large enough to steer current

# Current Steering DAC with Supply Independent Biasing



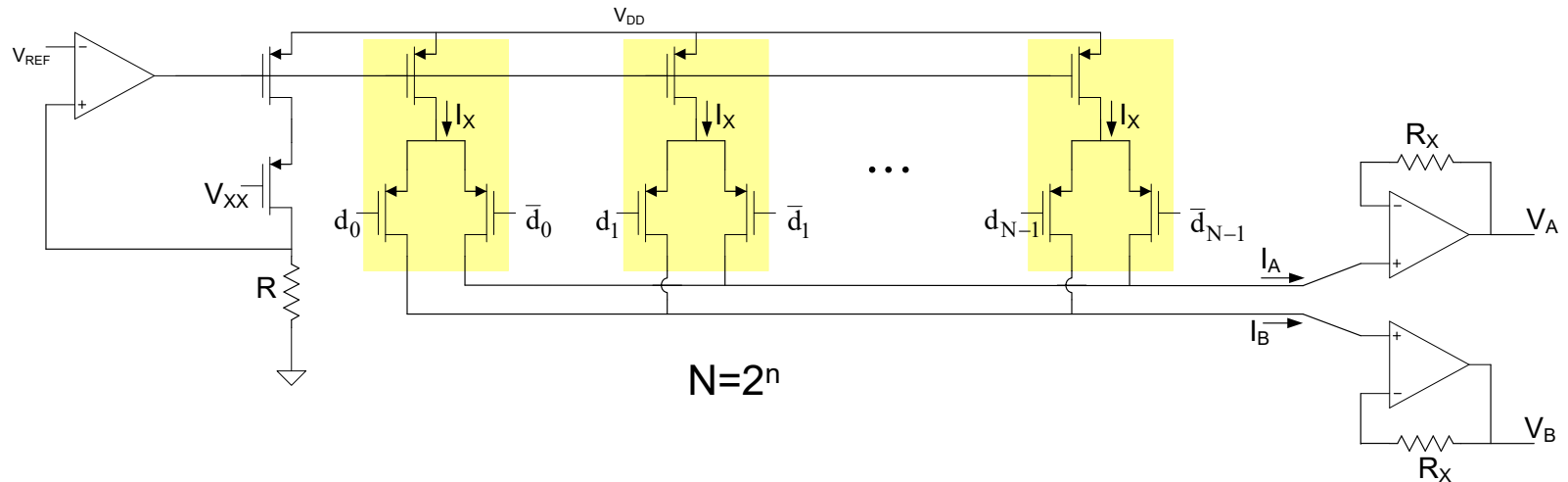
If transistors on top row are all matched,  $I_X = V_{REF}/R$

### Thermometer coded structure (requires binary to thermometer decoder)

$$I_A = \left( \frac{V_{REF}}{R} \right) \sum_{i=0}^{N-1} d_i$$

## Provides Differential Output Currents

# Current Steering DAC with Supply Independent Biasing

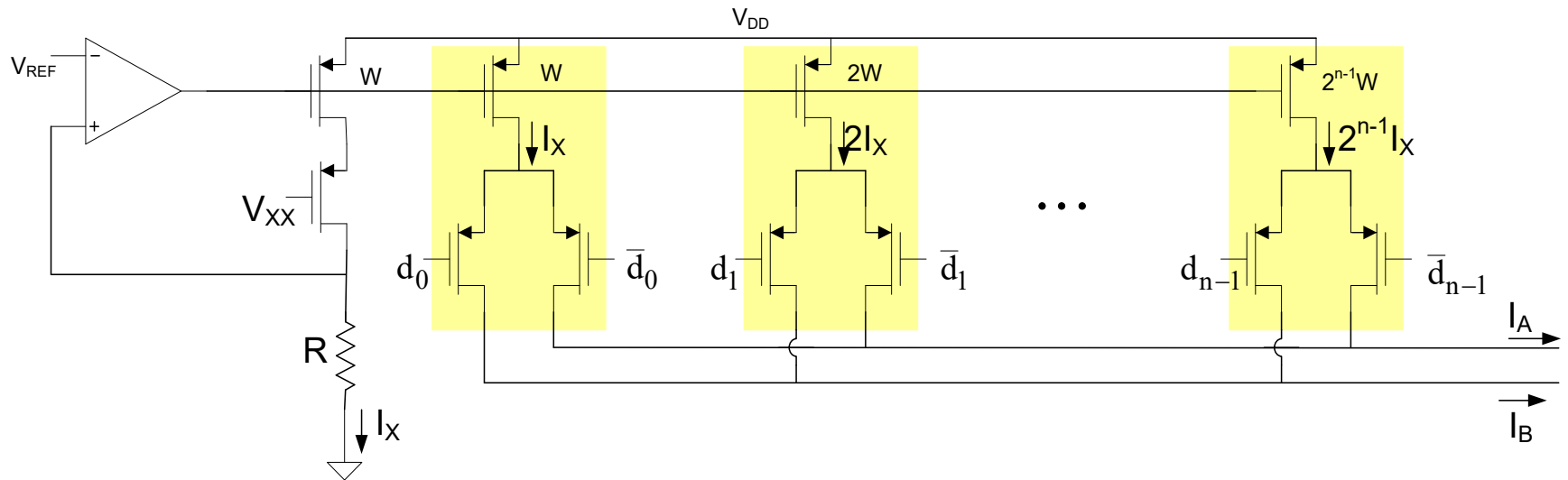


If transistors on top row are all matched,  $I_X = V_{REF}/R$

$$V_A = \left( -V_{REF} \frac{R_A}{R} \right) \sum_{i=0}^{N-1} d_i$$

Provides Differential Output Voltages

# Current Current Steering DAC with Supply Independent Biasing



If transistors on top row are binary weighted

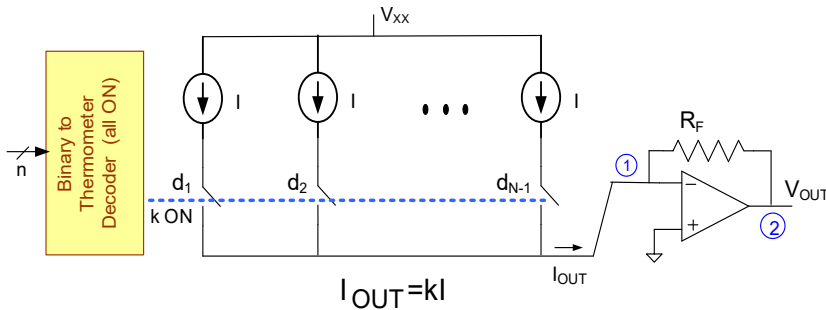
$$I_A = \left( \frac{V_{REF}}{R} \right) \sum_{i=0}^{n-1} \frac{d_i}{2^{n-i}}$$

Provides Differential Output Currents

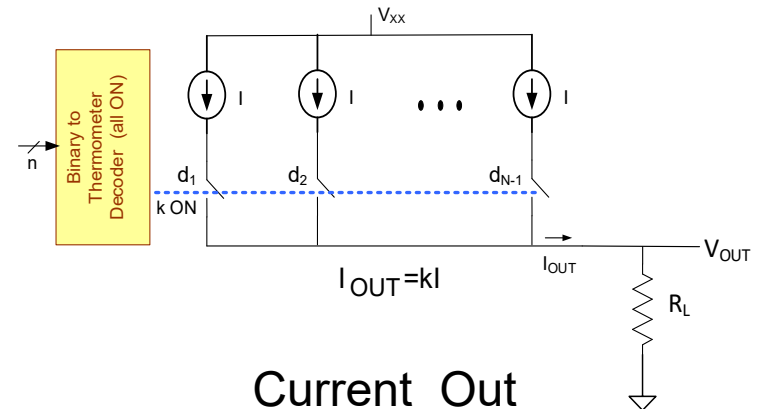
Does this serve as an MDAC?



# Current Steering DAC



Voltage Out



Current Out

- Many current steering DACs have an output current instead of an output voltage
- Output voltage is often established by steering current to a fixed external resistor (50 $\Omega$  or 100  $\Omega$ )
- Most basic current steering architectures with a high output impedance can be used by simply removing the op amp
- Whereas output impedance of current sources was not of major concern when driving a null-port, it can be of major concern for current output
- Speed may improve and power dissipation may decrease in internal circuitry if output is current



Stay Safe and Stay Healthy !

**End of Lecture 17**